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HP Gwen REV.A (HP SCH P/N:718773-000)

HP Mordred REV.A (HP SCH P/N:718773-000)

uATX(244 mm X 244 mm)

(MS-7860 12)

CPU:

Intel Haswell Processor

HP P/N	Description
718772-001	PCA,GWEN
718773-000	SCH,GWEN
718774-001	PCB,GWEN

System Chipset:

Intel Lynx Point Chipset

HP P/N	Description
718775-001	PCA,MORDRED
718773-000	SCH,MORDRED
718774-001	PCB,MORDRED

OnBoard Chipset:

AZALIA Codec: Realtek ALC 221

LAN: Realtek RTL8151GH-CG 10/100/1000 NIC

SIO: Nuvoton NPCD379H

Flash ROM: 64 Mb

Main Memory:

DDRIII (1333/1600MHz) * 4 (Dual Channel)

Expansion Slots:

PCI Express (X16) Slot * 1

PCI Express (X1) Slot * 3

DDI Port Slot *1

PWM:

Controller: ISL95816HRZ

Controller: NCP1587GDR2G

BOM DISTRIBUTION RULE

Gwen,Mordred

(BOM,BOM)

Other:

SATA *4

USB3.0 *5 (Rear*2 Front*2 Internal*1)

USB2.0 *8 (Rear*4 Front*2 Internal*2)

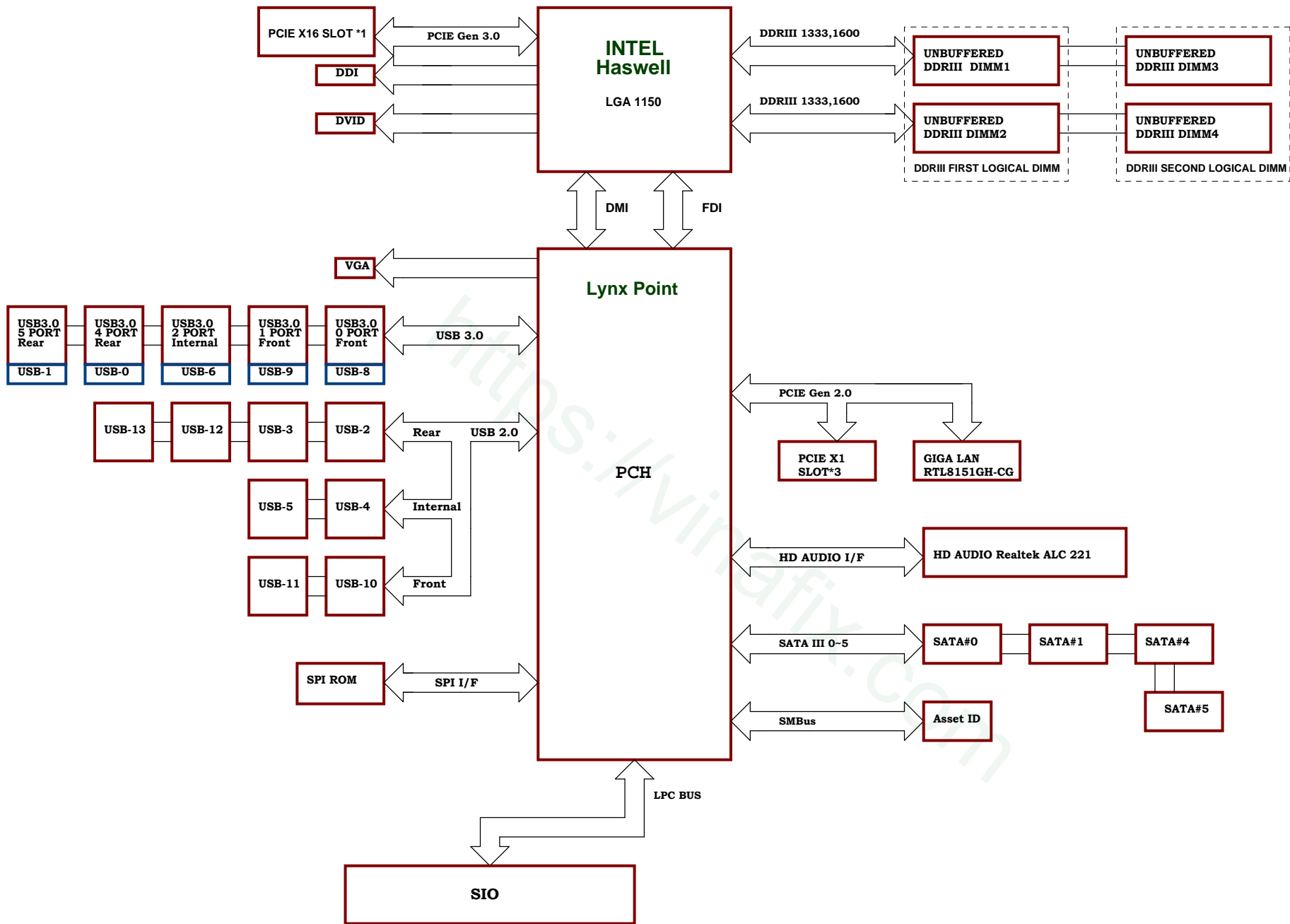
DVI PORT*1

VGA PORT *1

PRINT Header *1

COM PORT *1

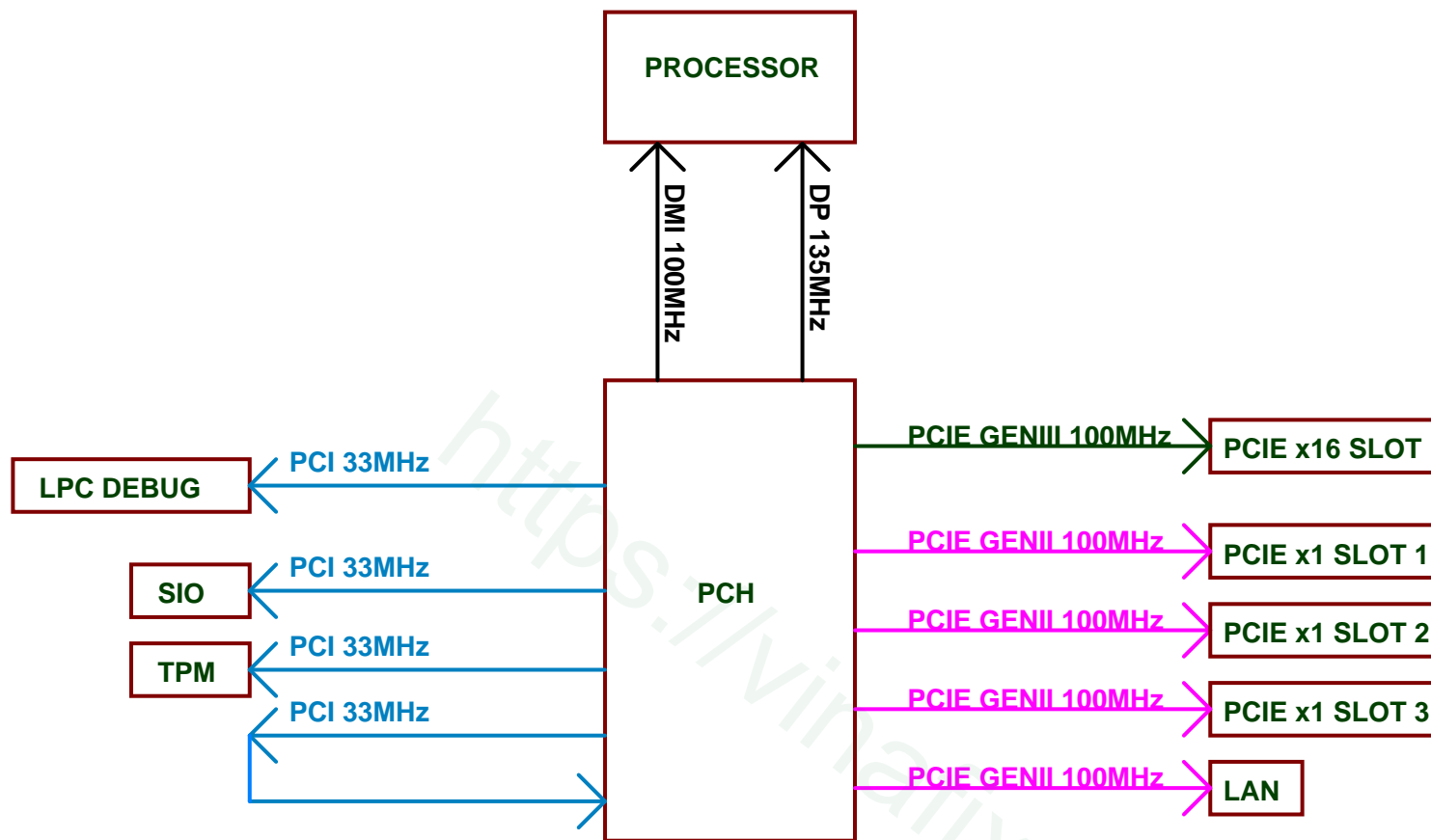
COM Header *1



Release Date : Wednesday, September 04, 2013

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MSI		MICRO-STAR INT'L CO.,LTD	
HP SCH P/N: 718773-000(MSI MS-7860)		Rev A	
Size Custom	Document Description	Block Diagram	
Date:	Sheet 2 of 56		

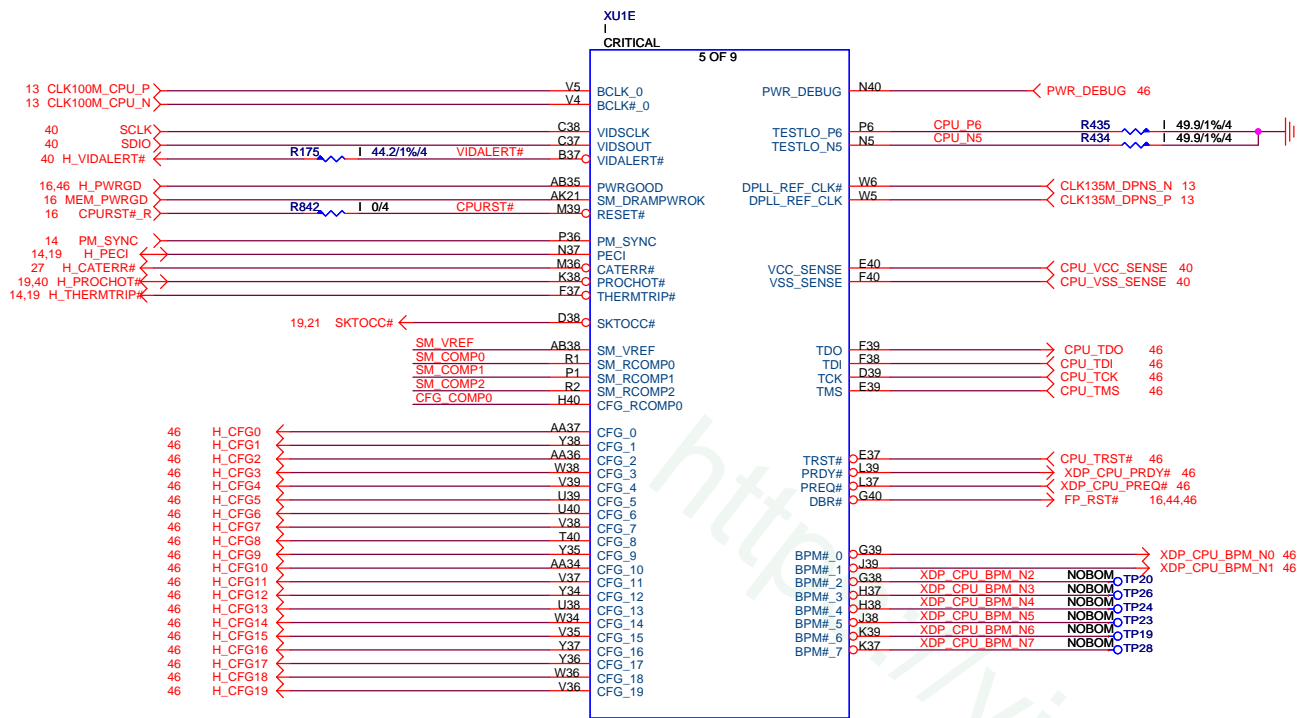


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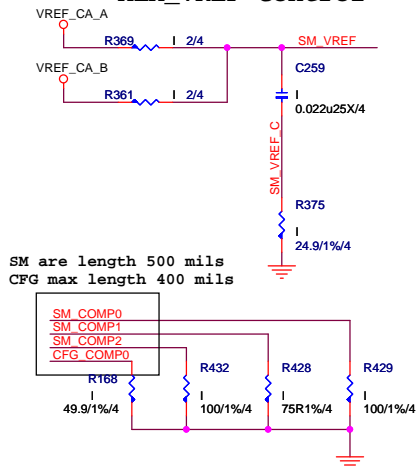
MICRO-STAR INT'L CO.,LTD		
HP SCH P/N: 718773-000(MSI MS-7860)		
Size Custom	Document Description Clock Distribution	Rev A
Date:	Sheet 3 of 56	



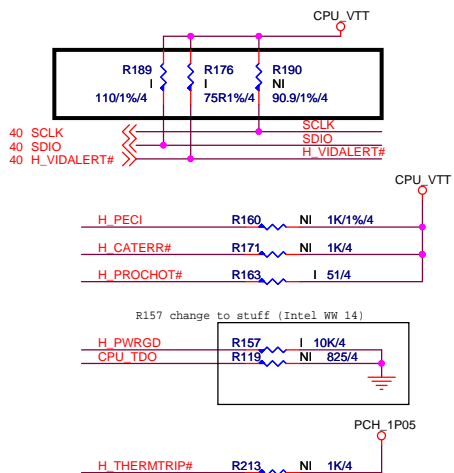
46 H_CFG[19..0] <-> H_CFG[19..0]

CPU2_2 N12-150A010-L06
AVL:N12-150A020-F02

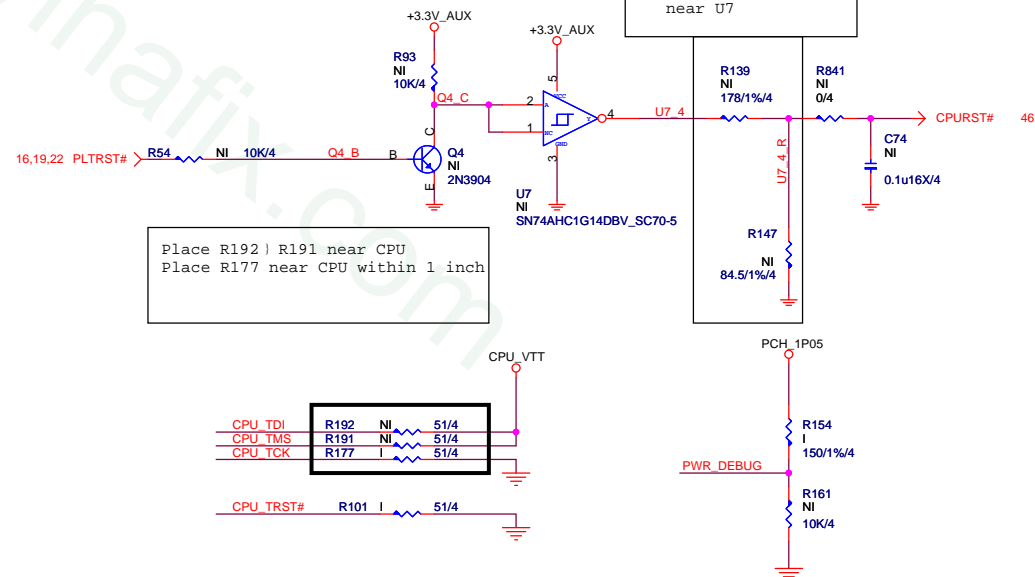
MEM_VREF Control



Place R189 | R176 | R190 near CPU



CPU_RESET#



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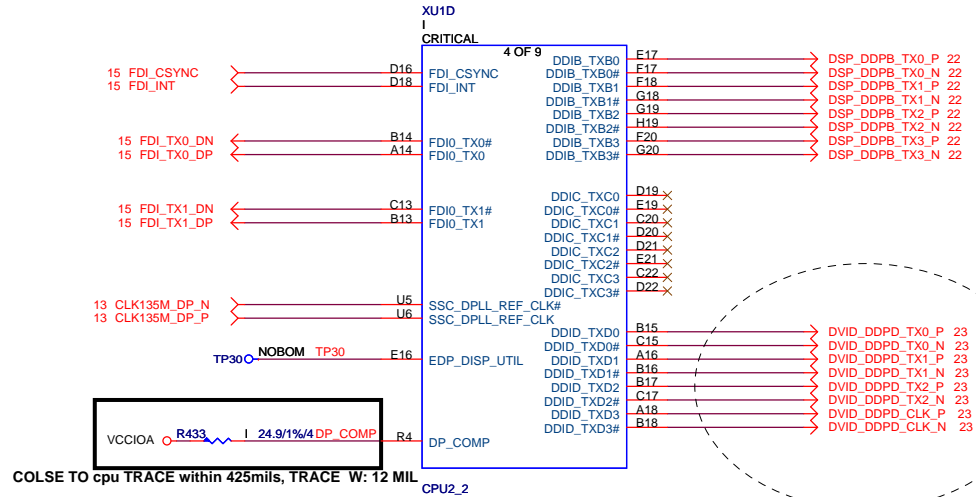
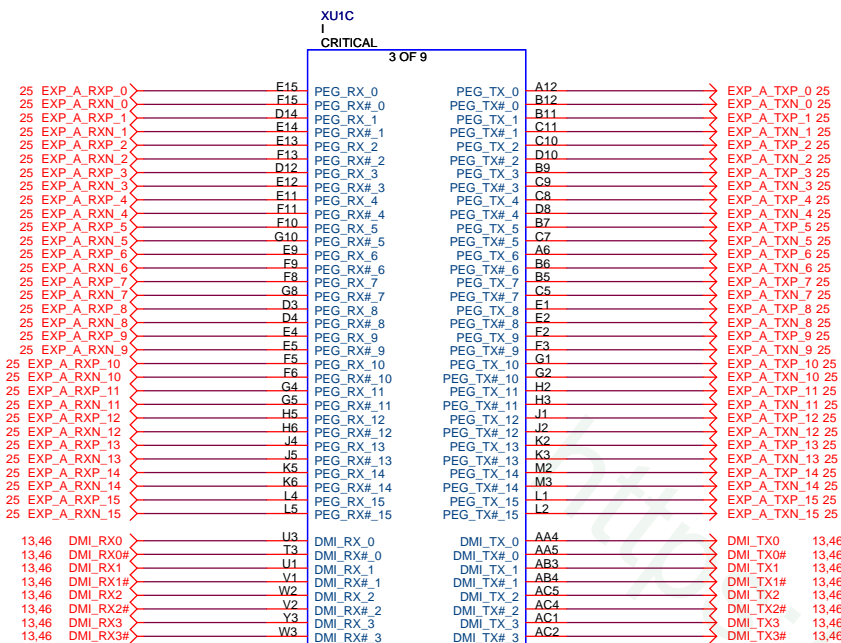
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Size	Document Description	Rev
Custom	CPU-CLK/Control	A
Date:	Sheet 4 of 56	




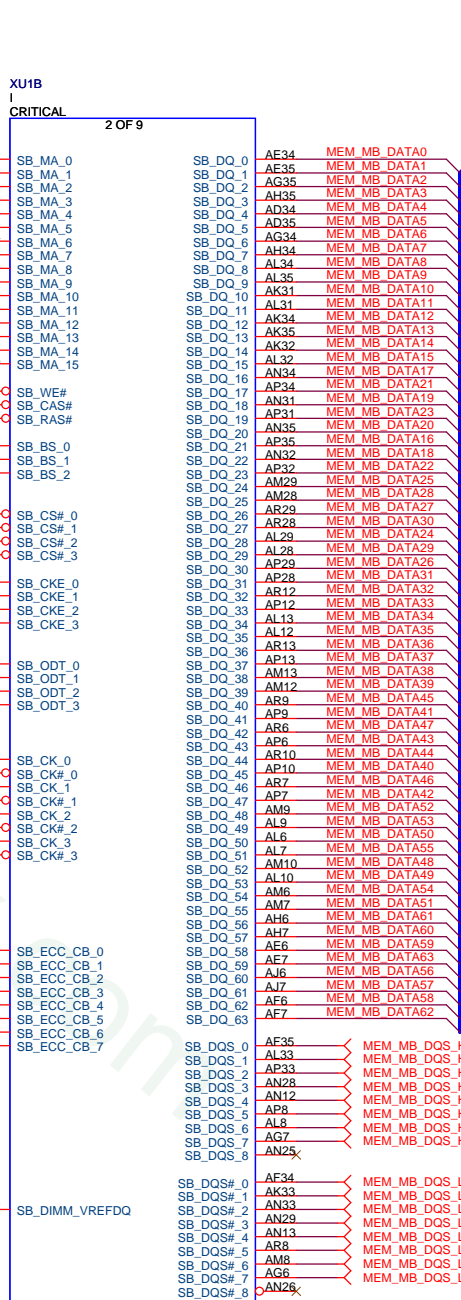
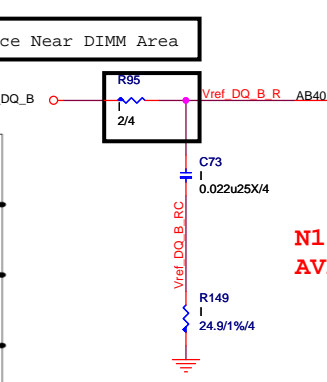
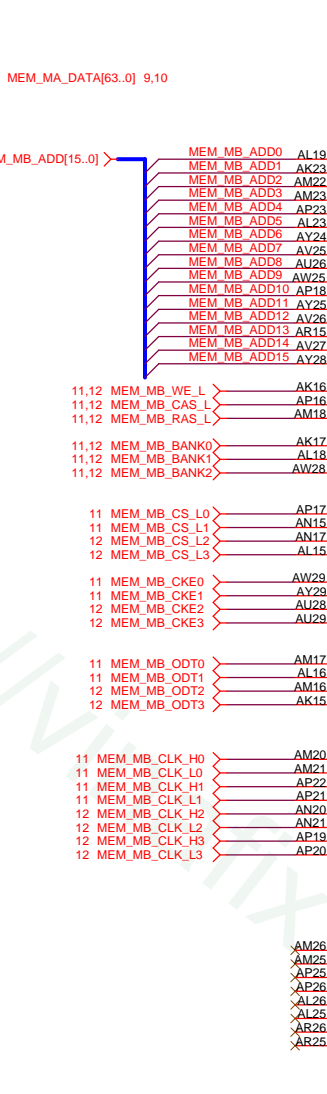
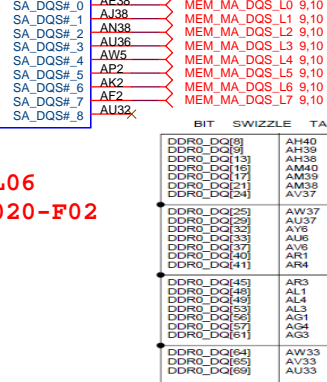
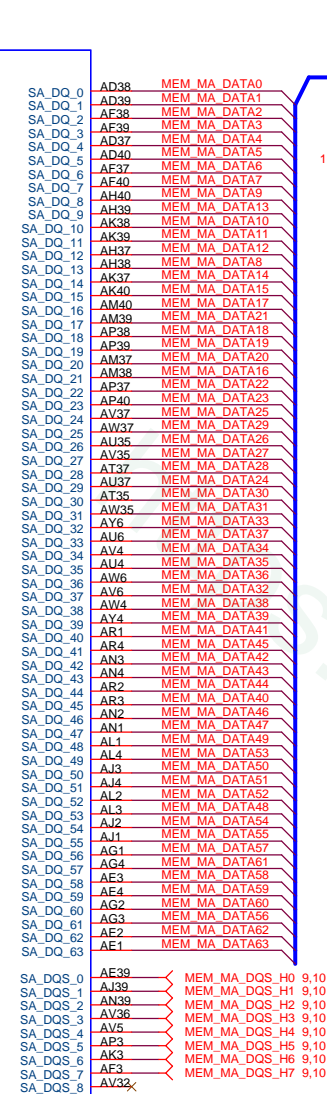
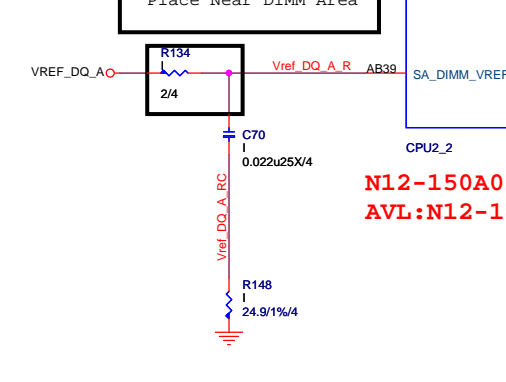
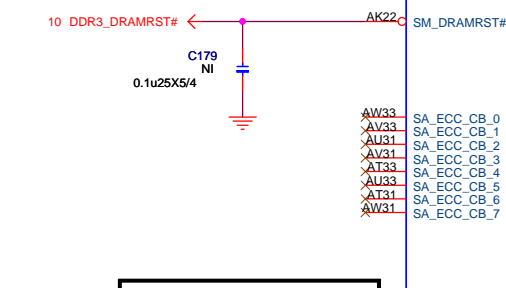
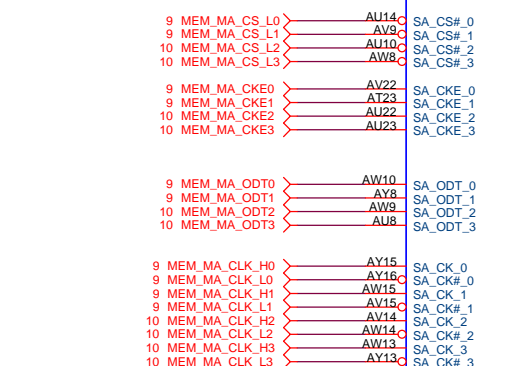
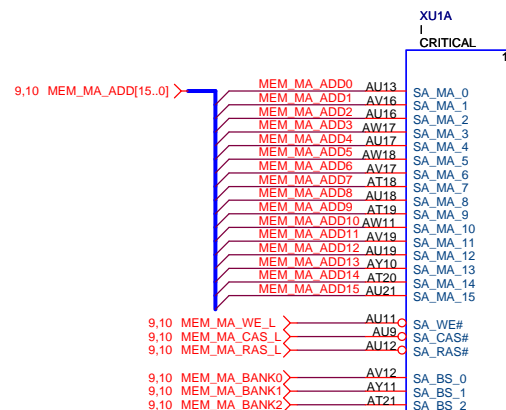
N12-150A010-L06
AVL:N12-150A020-F02

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			HP SCH P/N: 718773-000(MSI MS-7860)	
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	CPU-PEG/MISC			
Date:		Sheet	5	of 56

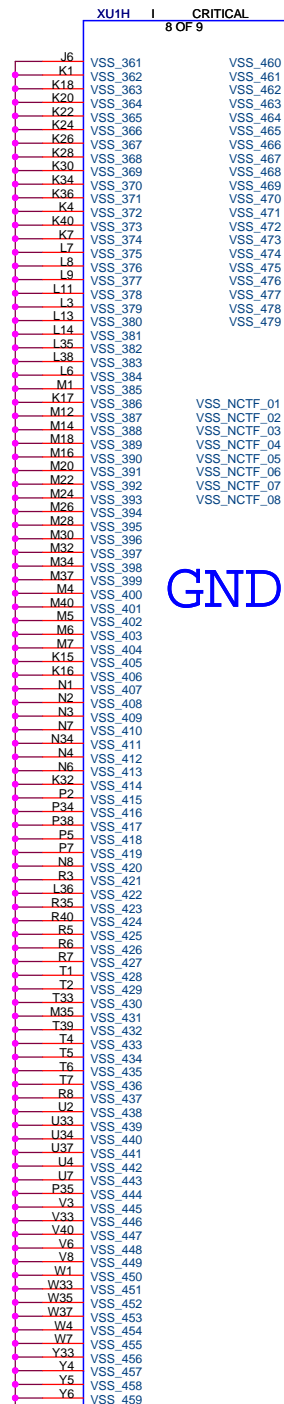


HSW DQ MAPPING TABLE

HSW PIN NAME	Pin#	MC DQ#
DDR1_DQ[0]	AE34	DQ 0
DDR1_DQ[1]	AE35	DQ 1
DDR1_DQ[2]	AG35	DQ 2
DDR1_DQ[3]	AH35	DQ 3
DDR1_DQ[4]	AD34	DQ 4
DDR1_DQ[5]	AG34	DQ 5
DDR1_DQ[6]	AK31	DQ 6
DDR1_DQ[7]	AL34	DQ 7
DDR1_DQ[8]	AL35	DQ 8
DDR1_DQ[9]	AK34	DQ 9
DDR1_DQ[10]	AK32	DQ 10
DDR1_DQ[11]	AN34	DQ 11
DDR1_DQ[12]	AP34	DQ 12
DDR1_DQ[13]	AN31	DQ 13
DDR1_DQ[14]	AK32	DQ 14
DDR1_DQ[15]	AL32	DQ 15
DDR1_DQ[16]	AP35	DQ 16
DDR1_DQ[17]	AN34	DQ 17
DDR1_DQ[18]	AN32	DQ 18
DDR1_DQ[19]	AN31	DQ 19
DDR1_DQ[20]	AN35	DQ 20
DDR1_DQ[21]	AP34	DQ 21
DDR1_DQ[22]	AP32	DQ 22
DDR1_DQ[23]	AP31	DQ 23
DDR1_DQ[24]	AL28	DQ 24
DDR1_DQ[25]	AM29	DQ 25
DDR1_DQ[26]	AM29	DQ 26
DDR1_DQ[27]	AP29	DQ 27
DDR1_DQ[28]	AM28	DQ 28
DDR1_DQ[29]	AL28	DQ 29
DDR1_DQ[30]	AR28	DQ 30
DDR1_DQ[31]	AP28	DQ 31
DDR1_DQ[32]	AR12	DQ 32
DDR1_DQ[33]	AP12	DQ 33
DDR1_DQ[34]	AL13	DQ 34
DDR1_DQ[35]	AL12	DQ 35
DDR1_DQ[36]	AP13	DQ 36
DDR1_DQ[37]	AP13	DQ 37
DDR1_DQ[38]	AM13	DQ 38
DDR1_DQ[39]	AM12	DQ 39
DDR1_DQ[40]	AP10	DQ 40
DDR1_DQ[41]	AP9	DQ 41
DDR1_DQ[42]	AP7	DQ 42
DDR1_DQ[43]	AP6	DQ 43
DDR1_DQ[44]	AR10	DQ 44
DDR1_DQ[45]	AR9	DQ 45
DDR1_DQ[46]	AR7	DQ 46
DDR1_DQ[47]	AR6	DQ 47
DDR1_DQ[48]	AM10	DQ 48
DDR1_DQ[49]	AL10	DQ 49
DDR1_DQ[50]	AL6	DQ 50
DDR1_DQ[51]	AM7	DQ 51
DDR1_DQ[52]	AM9	DQ 52
DDR1_DQ[53]	AL9	DQ 53
DDR1_DQ[54]	AM6	DQ 54
DDR1_DQ[55]	AL7	DQ 55
DDR1_DQ[56]	AJ6	DQ 56
DDR1_DQ[57]	AJ7	DQ 57
DDR1_DQ[58]	AF6	DQ 58
DDR1_DQ[59]	AE6	DQ 59
DDR1_DQ[60]	AE7	DQ 60
DDR1_DQ[61]	AE8	DQ 61
DDR1_DQ[62]	AJ7	DQ 62
DDR1_DQ[63]	AM28	DQ 63
DDR1_DQ[64]	AM25	DQ 64
DDR1_DQ[65]	AP25	DQ 65
DDR1_DQ[66]	AP26	DQ 66
DDR1_DQ[67]	AL26	DQ 67
DDR1_DQ[68]	AL25	DQ 68
DDR1_DQ[69]	AR26	DQ 69
DDR1_DQ[70]	AR25	DQ 70
DDR1_DQ[71]	AR25	DQ 71

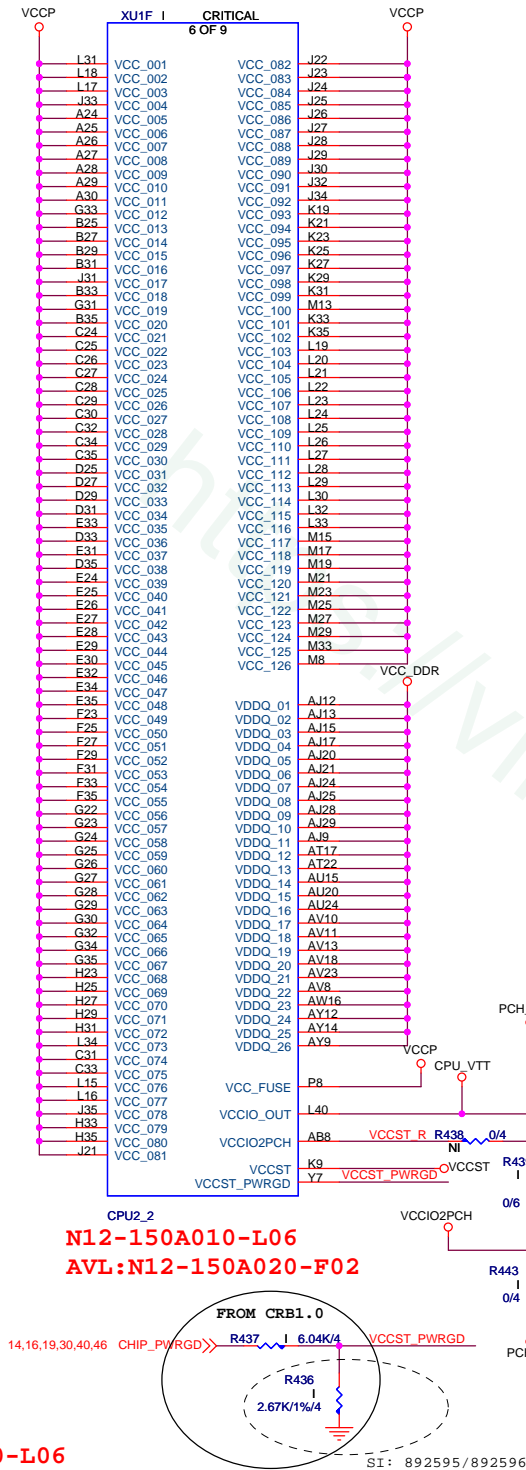
BIT SWIZZLE TABLE			
DDR0_DQ[8]	AH40	DQ 9	
DDR0_DQ[9]	AM39	DQ 13	
DDR0_DQ[10]	AH38	DQ 17	
DDR0_DQ[11]	AM40	DQ 21	
DDR0_DQ[12]	AM39	DQ 25	
DDR0_DQ[13]	AV37	DQ 29	
DDR0_DQ[25]	AW37	DQ 33	
DDR0_DQ[26]	AU37	DQ 37	
DDR0_DQ[27]	AY6	DQ 41	
DDR0_DQ[28]	AY6	DQ 45	
DDR0_DQ[29]	AY6	DQ 49	
DDR0_DQ[30]	AR1	DQ 53	
DDR0_DQ[31]	AR4	DQ 57	
DDR0_DQ[45]	AR3	DQ 61	
DDR0_DQ[46]	AL1	DQ 65	
DDR0_DQ[47]	AL4	DQ 69	
DDR0_DQ[53]	AL3	DQ 73	
DDR0_DQ[54]	AG1	DQ 77	
DDR0_DQ[55]	AG4	DQ 81	
DDR0_DQ[56]	AG3	DQ 85	
DDR0_DQ[64]	AW33	DQ 89	
DDR0_DQ[65]	AV33	DQ 93	
DDR0_DQ[66]	AU33	DQ 97	



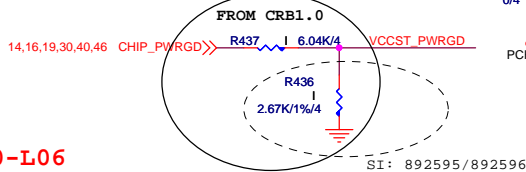


GND

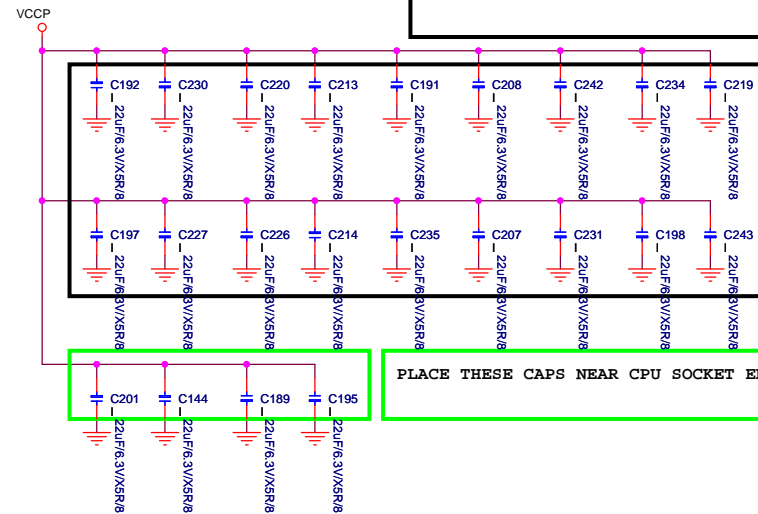
N12-150A010-L06
AVL:N12-150A020-F02



CPU2_2
N12-150A010-L06
AVL:N12-150A020-F02

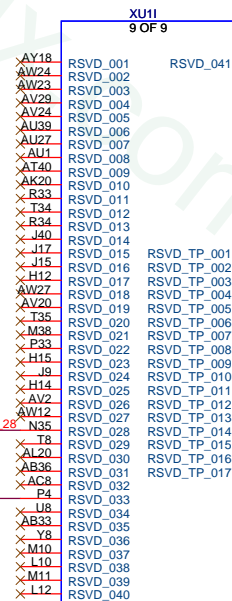
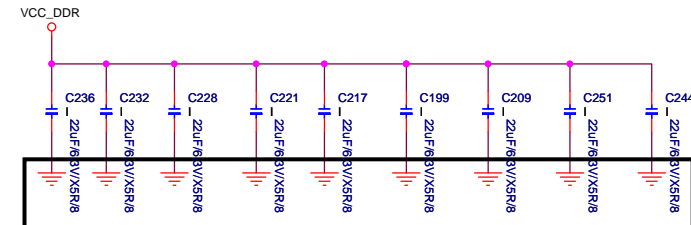


VCCP-Decoupling



PLACE THESE CAPS NEAR CPU SOCKET EDGE

VCC_DDR-Decoupling



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Custom	CPU-GND/Power	A
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XU1G
CRITICAL

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GND

N12-150A010-L06

AVL:N12-150A020-F02

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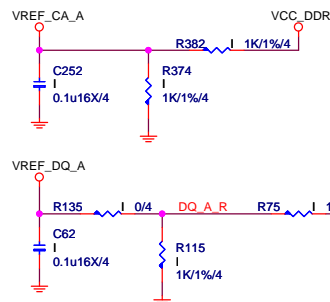


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Size Custom	Document Description CPU-GND	Rev A
Date:	Sheet 8 of 56	

DDRIII DIMM_A1

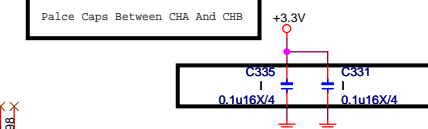
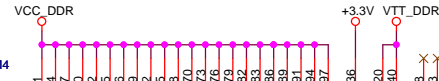
WHITE COLOR
N13-2401611-F02

6,10 MEM_MA_DATA[63..0] ← MEM_MA_DATA[63..0]



MEM_MA_DATA0_3
MEM_MA_DATA1_4
MEM_MA_DATA2_9
MEM_MA_DATA3_10
MEM_MA_DATA4_122
MEM_MA_DATA5_123
MEM_MA_DATA6_128
MEM_MA_DATA7_129
MEM_MA_DATA8_12
MEM_MA_DATA9_13
MEM_MA_DATA10_18
MEM_MA_DATA11_19
MEM_MA_DATA12_31
MEM_MA_DATA13_32
MEM_MA_DATA14_37
MEM_MA_DATA15_38
MEM_MA_DATA16_21
MEM_MA_DATA17_22
MEM_MA_DATA18_27
MEM_MA_DATA19_28
MEM_MA_DATA20_40
MEM_MA_DATA21_41
MEM_MA_DATA22_46
MEM_MA_DATA23_47
MEM_MA_DATA24_30
MEM_MA_DATA25_31
MEM_MA_DATA26_36
MEM_MA_DATA27_37
MEM_MA_DATA28_49
MEM_MA_DATA29_50
MEM_MA_DATA30_55
MEM_MA_DATA31_56
MEM_MA_DATA32_61
MEM_MA_DATA33_62
MEM_MA_DATA34_87
MEM_MA_DATA35_88
MEM_MA_DATA36_200
MEM_MA_DATA37_201
MEM_MA_DATA38_206
MEM_MA_DATA39_207
MEM_MA_DATA40_90
MEM_MA_DATA41_91
MEM_MA_DATA42_96
MEM_MA_DATA43_97
MEM_MA_DATA44_99
MEM_MA_DATA45_210
MEM_MA_DATA46_215
MEM_MA_DATA47_216
MEM_MA_DATA48_99
MEM_MA_DATA49_100
MEM_MA_DATA50_105
MEM_MA_DATA51_106
MEM_MA_DATA52_118
MEM_MA_DATA53_219
MEM_MA_DATA54_224
MEM_MA_DATA55_225
MEM_MA_DATA56_108
MEM_MA_DATA57_109
MEM_MA_DATA58_114
MEM_MA_DATA59_115
MEM_MA_DATA60_227
MEM_MA_DATA61_228
MEM_MA_DATA62_233
MEM_MA_DATA63_234

XMM4
INI
CRITICAL



MEM_MA_ADD0
MEM_MA_ADD1
MEM_MA_ADD2
MEM_MA_ADD3
MEM_MA_ADD4
MEM_MA_ADD5
MEM_MA_ADD6
MEM_MA_ADD7
MEM_MA_ADD8
MEM_MA_ADD9
MEM_MA_ADD10
MEM_MA_ADD11
MEM_MA_ADD12
MEM_MA_ADD13
MEM_MA_ADD14
MEM_MA_ADD15

MEM_MA_DQS_H0
MEM_MA_DQS_L0
MEM_MA_DQS_H1
MEM_MA_DQS_L1
MEM_MA_DQS_H2
MEM_MA_DQS_L2
MEM_MA_DQS_H3
MEM_MA_DQS_L3
MEM_MA_DQS_H4
MEM_MA_DQS_L4
MEM_MA_DQS_H5
MEM_MA_DQS_L5
MEM_MA_DQS_H6
MEM_MA_DQS_L6
MEM_MA_DQS_H7
MEM_MA_DQS_L7

MEM_MA_ODT0
MEM_MA_ODT1
MEM_MA_CKE0
MEM_MA_CKE1
MEM_MA_CS_L0
MEM_MA_CS_L1
MEM_MA_BANK0
MEM_MA_BANK1
MEM_MA_BANK2

MEM_MA_WE_L
MEM_MA_RAS_L
MEM_MA_CAS_L
MEM_MA_DRAMRST#_CHA
MEM_MA_CLK_H0
MEM_MA_CLK_L0
MEM_MA_CLK_H1
MEM_MA_CLK_L1

VREF_DQ_A
VREF_CA_A
SMBCLK_DDR
SMBDATA_DDR

VREF_DQ_A
VREF_CA_A
SMBCLK_DDR
SMBDATA_DDR

DDRIII-240P_WHITE-RH-2
XMM4(CHANNEL-A)
ADDRESS = 1:1 [SA1:SA0]

DDR3

10,11,12 SMBCLK_DDR ← SMBCLK_DDR R482 33/4 → SMB_CLK_MAIN 16,19,46
10,11,12 SMBDATA_DDR ← SMBDATA_DDR R485 33/4 → SMB_DATA_MAIN 16,19,46

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DDRIII DIMM_B1

WHITE COLOR
N13-2401611-F02

DDR3

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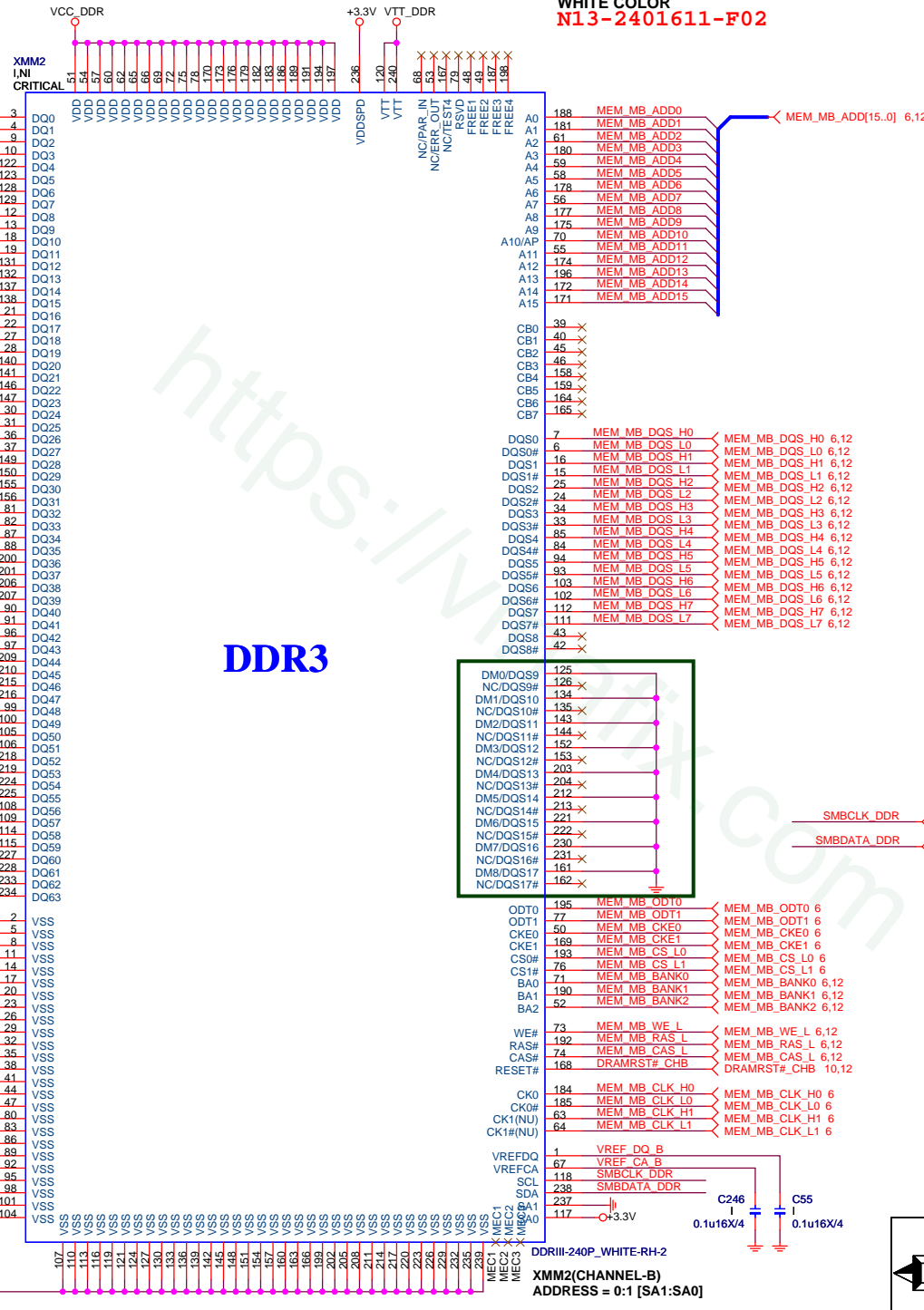
HP SCH P/N: 718773-000(MSI MS-7860)

Size	Document Description	Rev
Custom	DDR III XMM2	A
Date:	Sheet 11 of 56	



DDRIII-240P_WHITE-RH-2

XMM2(CHANNEL-B)
ADDRESS = 0:1 [SA1:SA0]



DDR +3.3V VTT_DDR

188 MEM_MB_ADD0 MEM_MB_ADD1 MEM_MB_ADD[15..0] 6,11



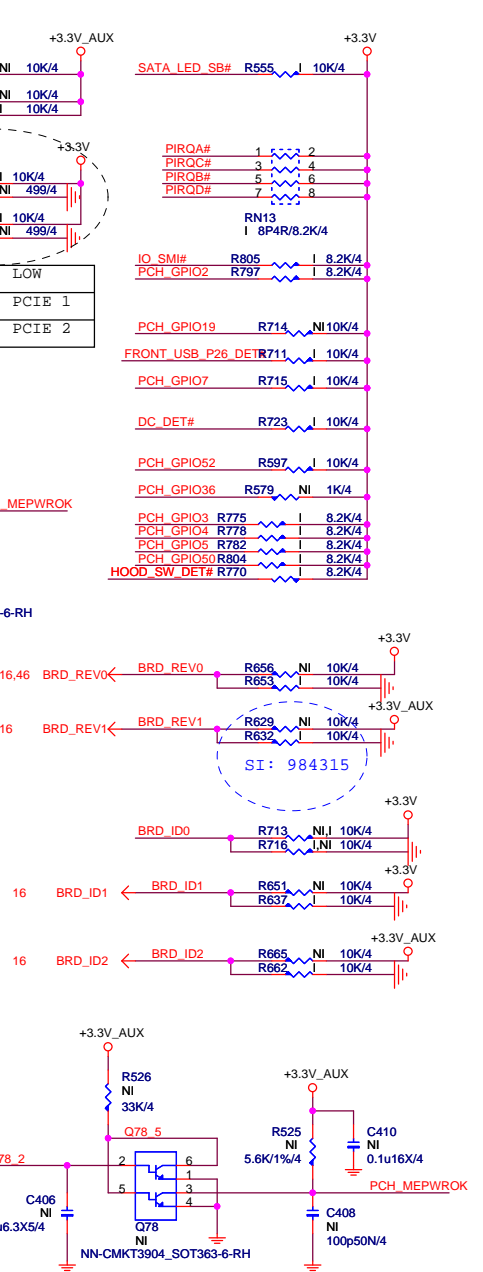
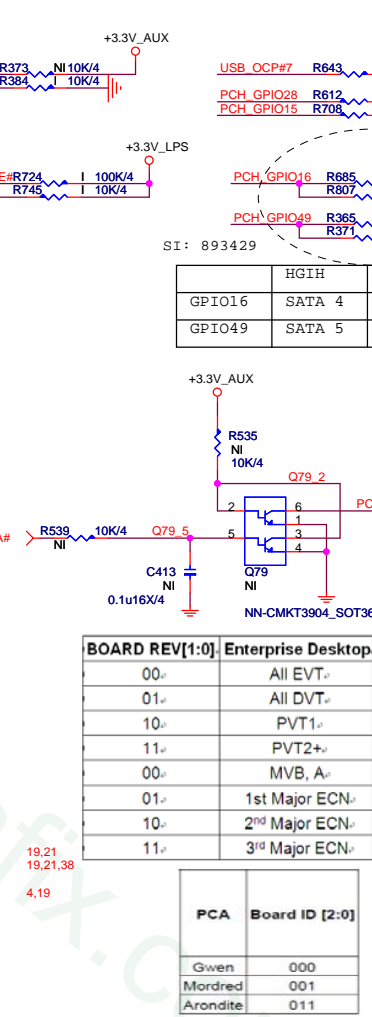
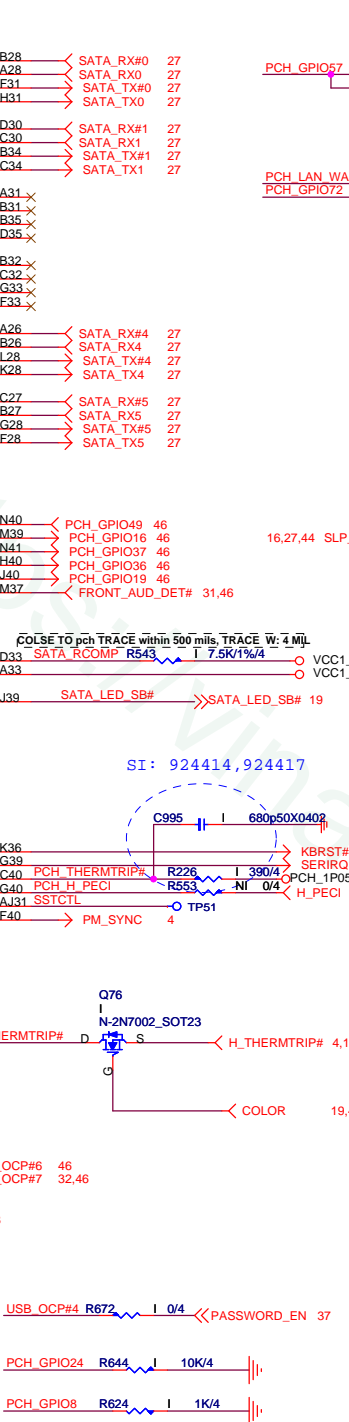
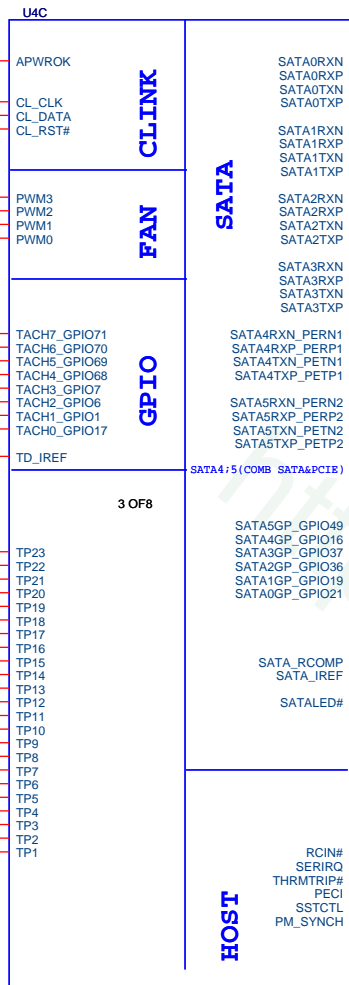
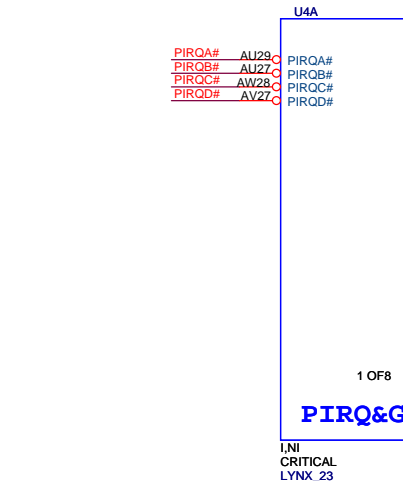
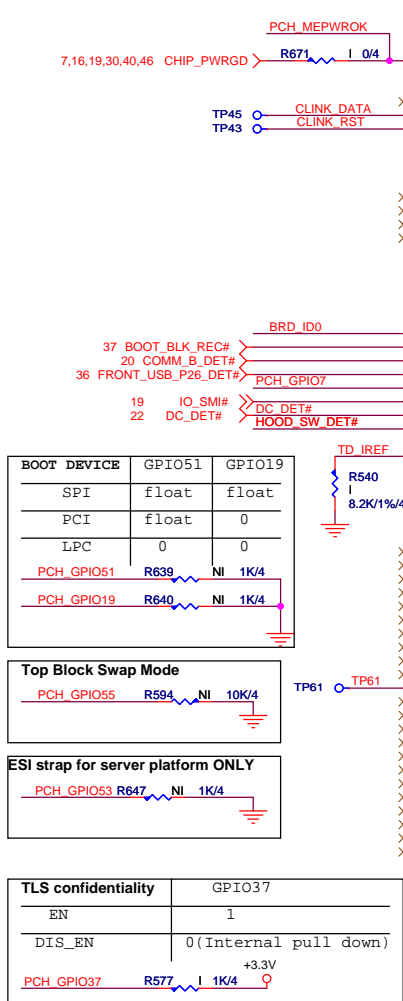
MICRO-STAR INT'L CO.,LTD

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Size Custom	Document Description DDR III XMM1
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Date:	Sheet 12 of 56
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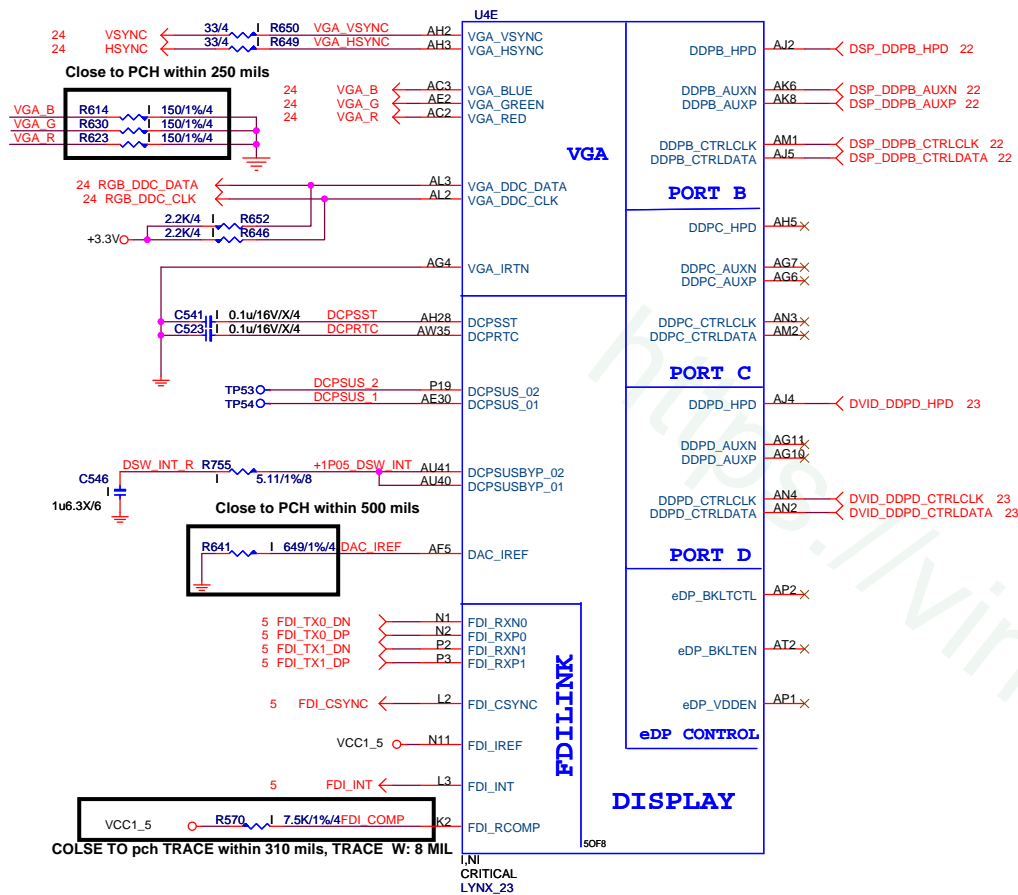




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PCH-SATA/HOST/GPIO			
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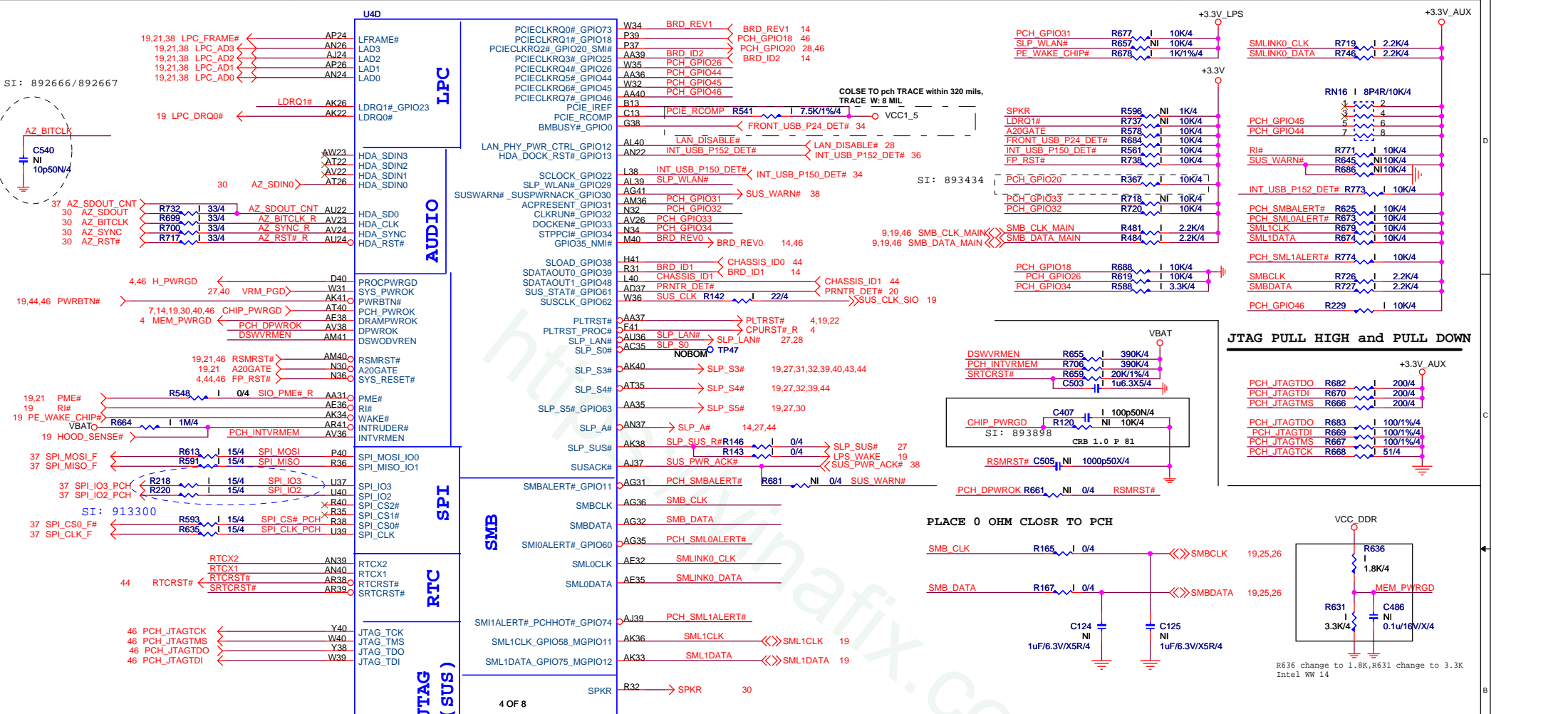


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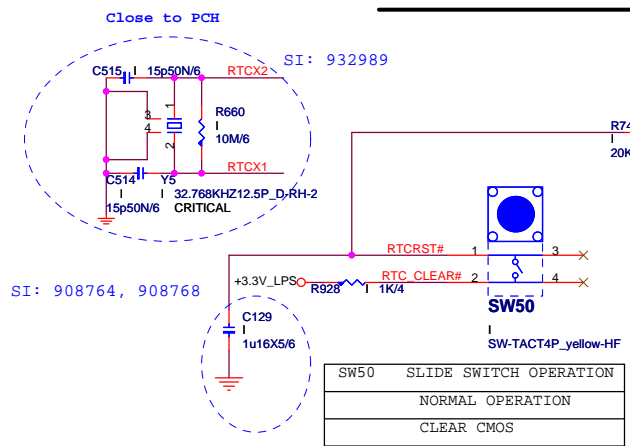
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Size Custom	Document Description PCH-DDI/VGA	Rev A
Date:	Sheet 15 of 56	

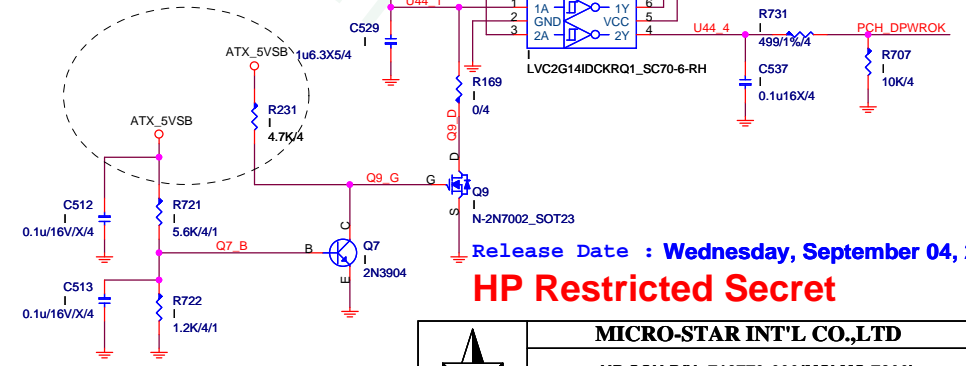


RTC Block



N91-01F0201-L06

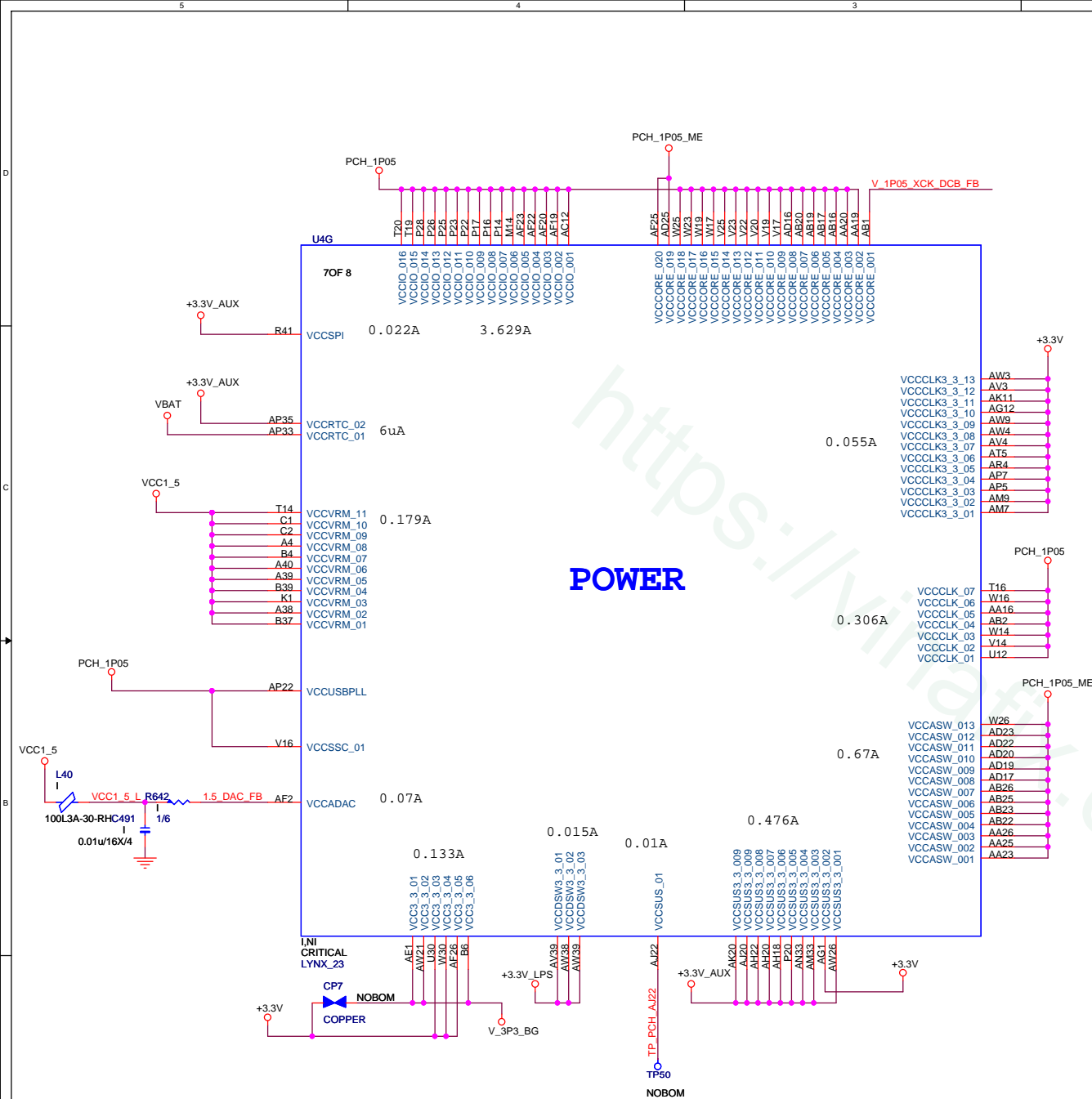
SI: 892601/892602



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Size Custom	Document Description	Rev A
PCH-SMB/LPC/AUDIO/RTC		
Date:	Sheet 16	of 56



Place C283\ C237 near P14, P16, P17,P26, P28
C285 near M14 C288 near U12 C289 near W14
C291 near AB2 C295 near V16 C297 near AA16, W16
C300 near AP22, AF19

Place C303 near AV4, AR4, AT5, AP5
C634 near AG1 C633 near W30 C304 near AF26

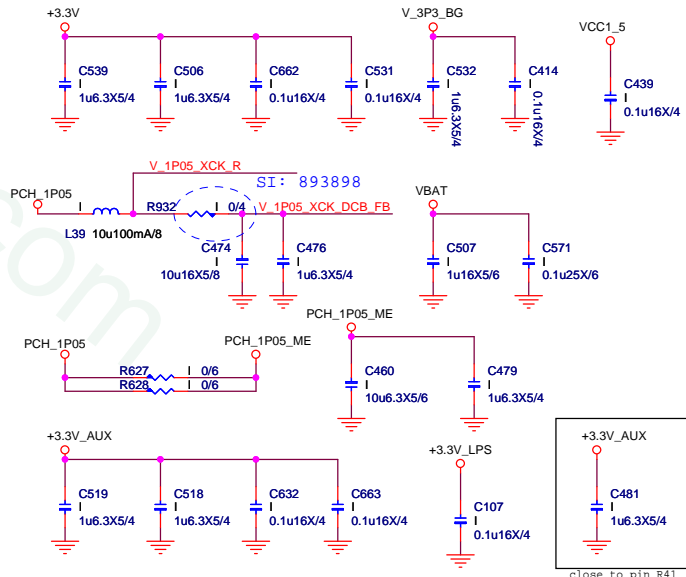
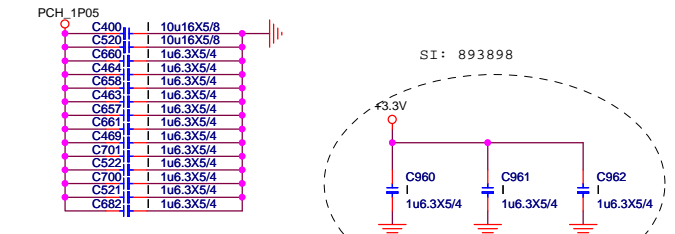
Place C630 near AN33 C301 near AK20
C631 near AW26 C302 near AP35

Place C635 near T14

Place C636 near AW39

Place C312\ C311 near AD17, AD19

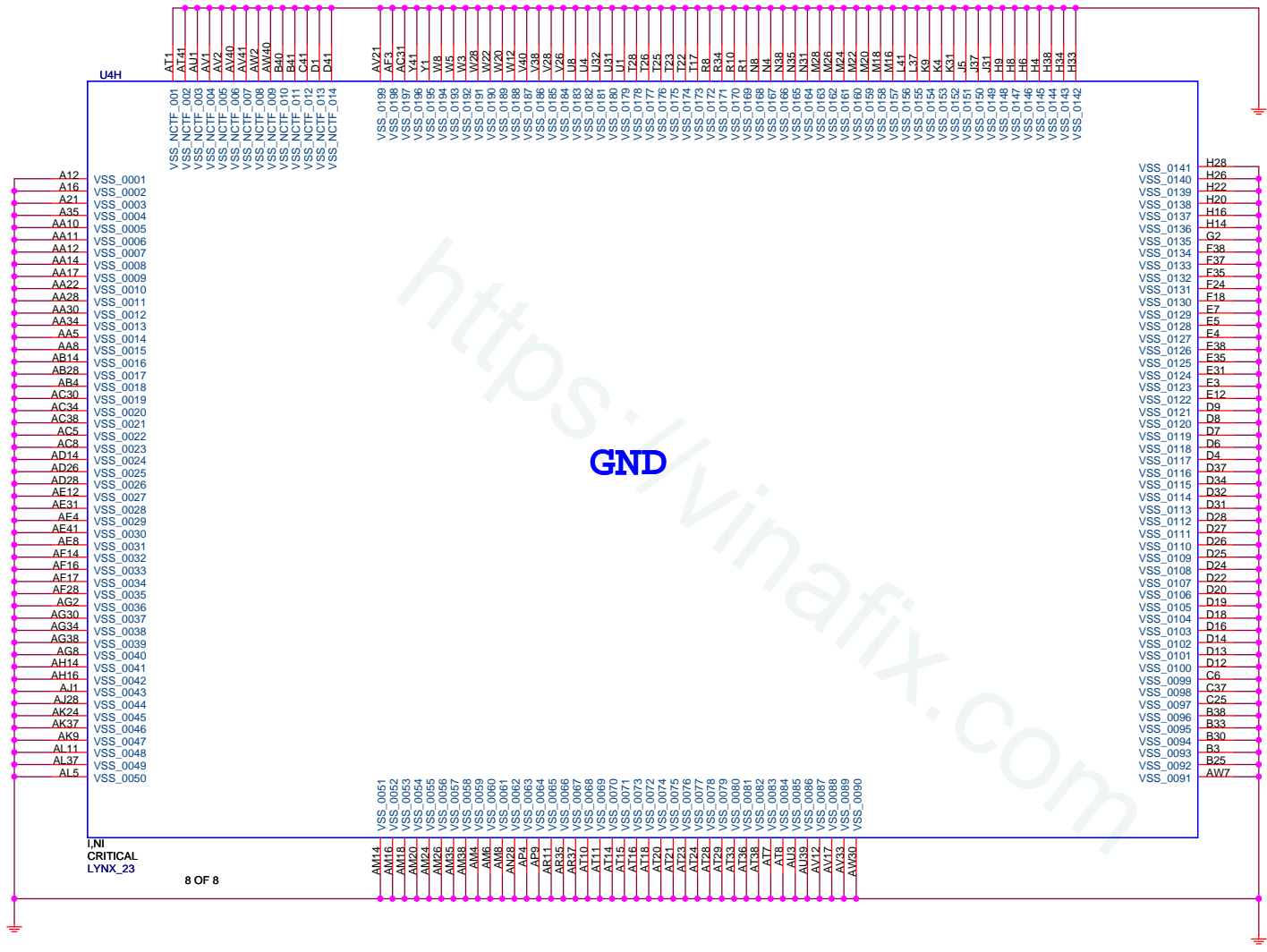
Place C306 near AW21 C632 near B6



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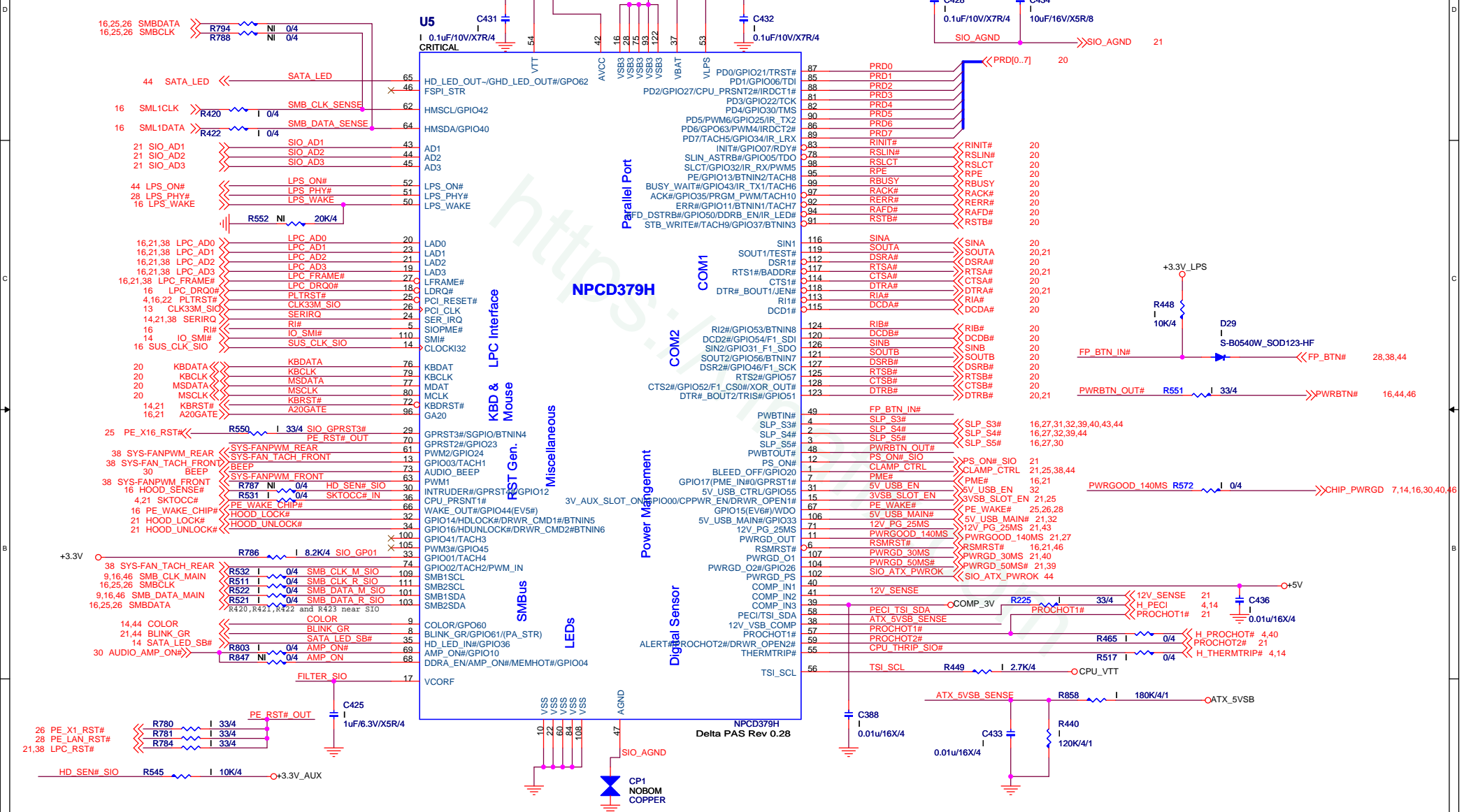


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Size Custom	Document Description	Rev A
PCH-GND		
Date:	Sheet 18 of 56	

LPC length should be less than 18 inches.

LPC SUPER I/O NPCD 379H

PN:B02-0379H04-NX9



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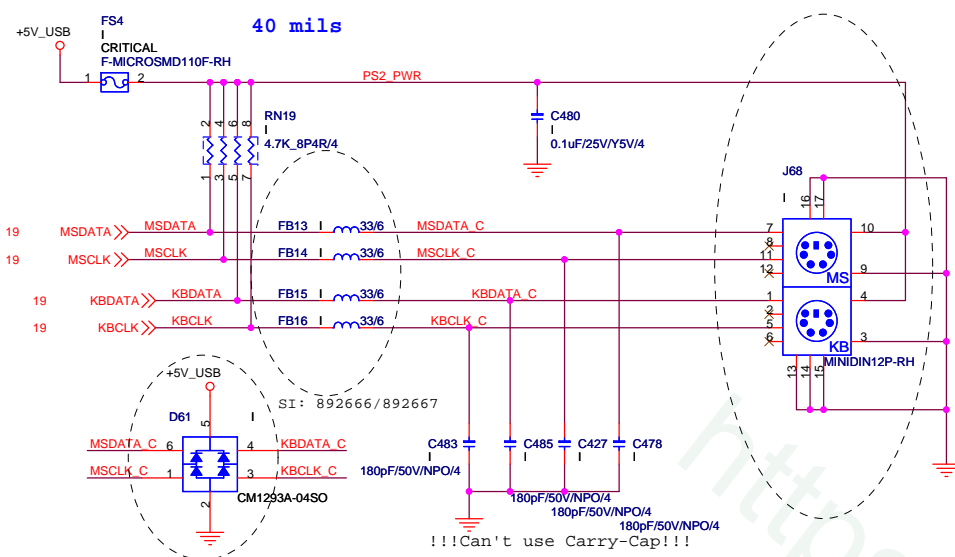


MICRO-STAR INT'L CO.,LTD

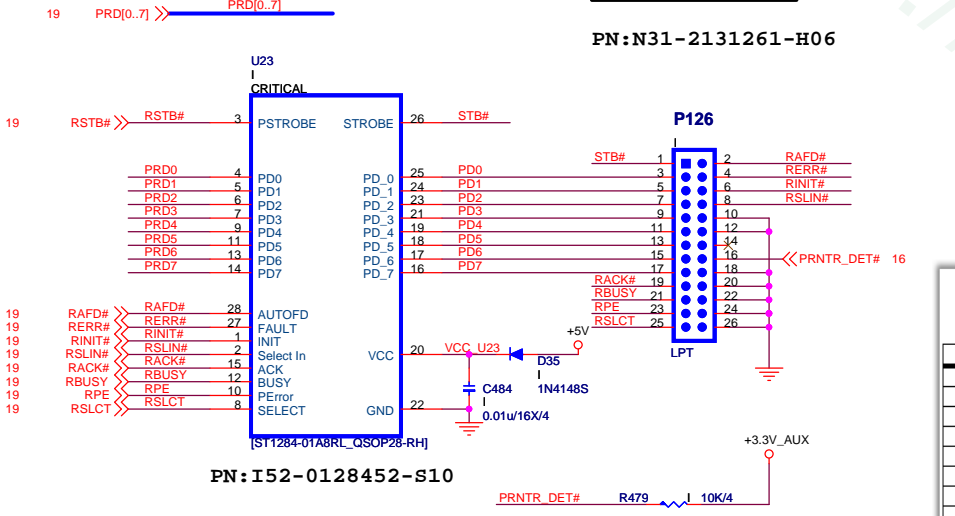
HP SCH P/N: 718773-000(MSI MS-7860)

Size	Document Description	Rev
Custom	SIO12-NPCD379H	A
Date:		

PS2 KEYBOARD & MOUSE CONNECTOR



PARALLEL PORT

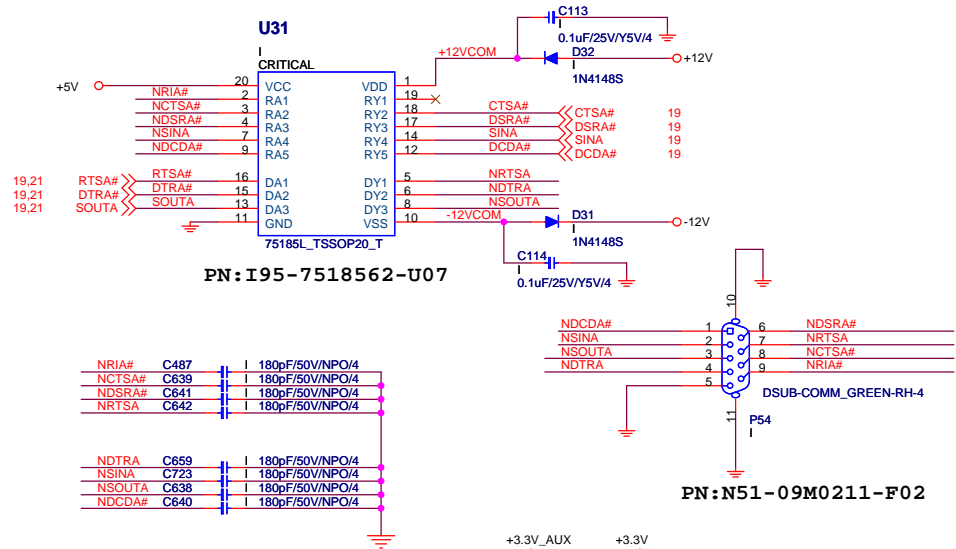


Parallel Port 2x13 header

PIN #	SIGNAL NAME	SIGNAL NAME	PIN #
1	LPT_STB#	XAFD#	2
3	LPT_SPD0	ERROR#	4
5	LPT_SPD1	XINIT#	6
7	LPT_SPD2	XSLIN#	8
9	LPT_SPD3	GND	10
11	LPT_SPD4	GND	12
13	LPT_SPD5	GND	14
15	LPT_SPD6	PRT_DET#	16
17	LPT_SPD7	GND	18
19	ACK#	GND	20
21	BUSY	GND	22
23	PE	LDT_RST#	24
	SLCT	GND	26

- PD0 C721 NI 180pF/50V/NPO/4
- PD1 C668 NI 180pF/50V/NPO/4
- PD2 C718 NI 180pF/50V/NPO/4
- PD3 C719 NI 180pF/50V/NPO/4
- PD4 C720 NI 180pF/50V/NPO/4
- PD5 C722 NI 180pF/50V/NPO/4
- PD6 C664 NI 180pF/50V/NPO/4
- PD7 C717 NI 180pF/50V/NPO/4
- STB# C716 NI 180pF/50V/NPO/4
- RACK# C704 NI 180pF/50V/NPO/4
- RBUSY C712 NI 180pF/50V/NPO/4
- RPE C713 NI 180pF/50V/NPO/4
- RSLCT C714 NI 180pF/50V/NPO/4
- RAFD# C715 NI 180pF/50V/NPO/4
- RERR# C681 NI 180pF/50V/NPO/4
- RSLIN# C708 NI 180pF/50V/NPO/4

SERIAL PORT 1



SERIAL PORT 2

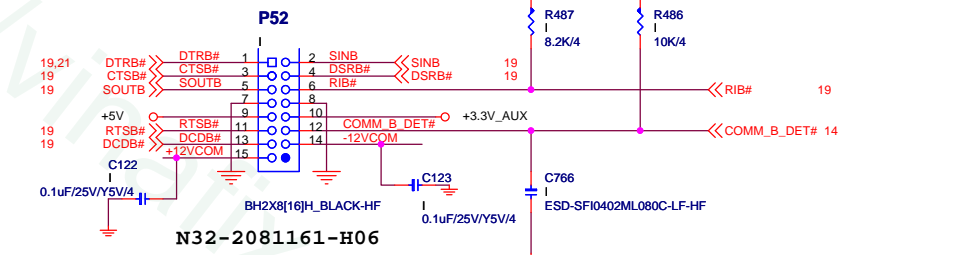
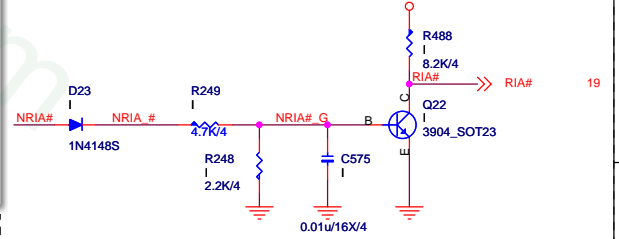


TABLE 12
FLOATING SERIAL PORT PIN DEFINITION (TOP VIEW)

Pin #	Signal Name	Signal Name	Pin #
1	DTR#	RXD	2
3	CTS#	DSR#	4
5	TXD	RI#	6
7	GND	GND	8
9	+5 V	+3.3 VAUX	10
11	RTS#	COMM B DETECT#	12
13	DCD#	-12 V (THRU DIODE)	14
15	+12 V (THRU DIODE)	KEY	16

Support ring wake up



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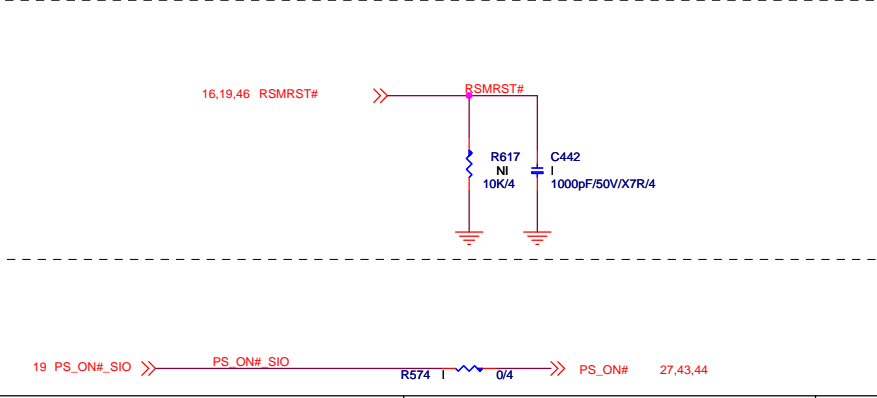
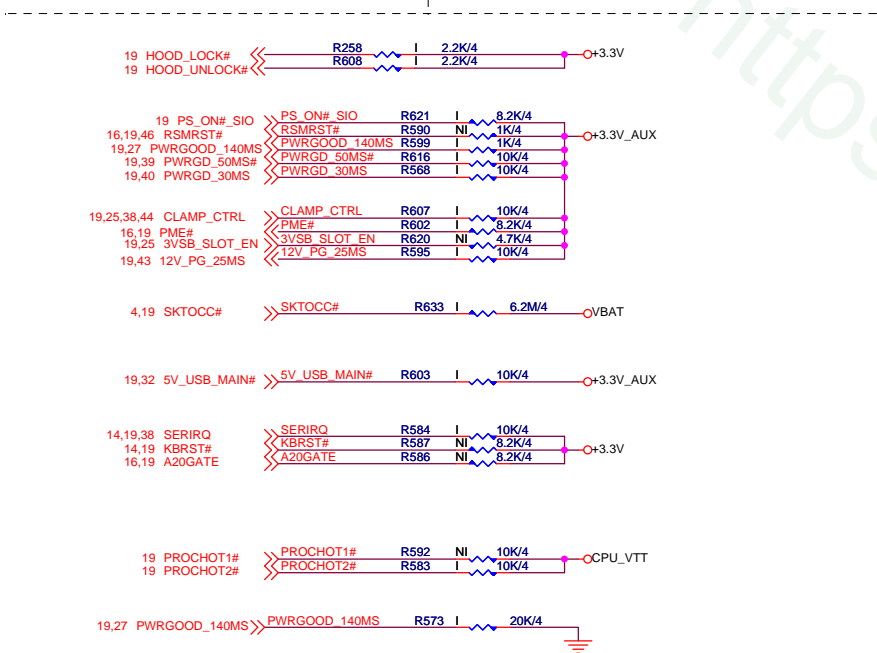
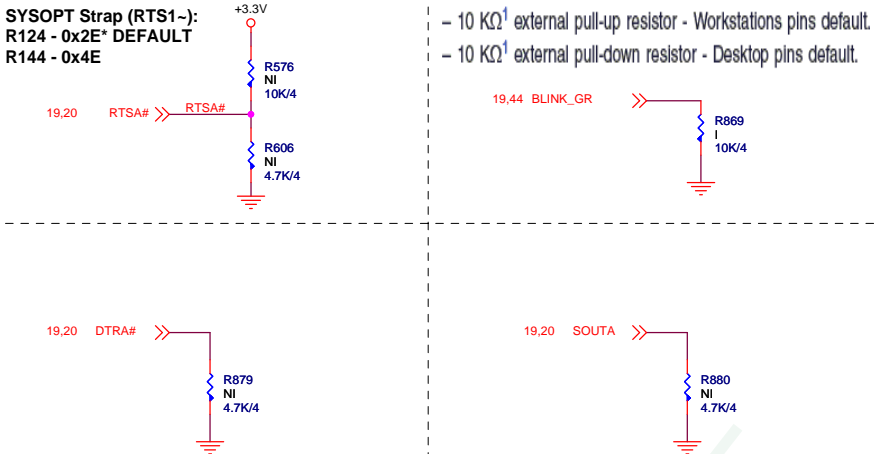
MICRO-STAR INT'L CO.,LTD

HP SCH P/N: 718773-000(MSI MS-7860)

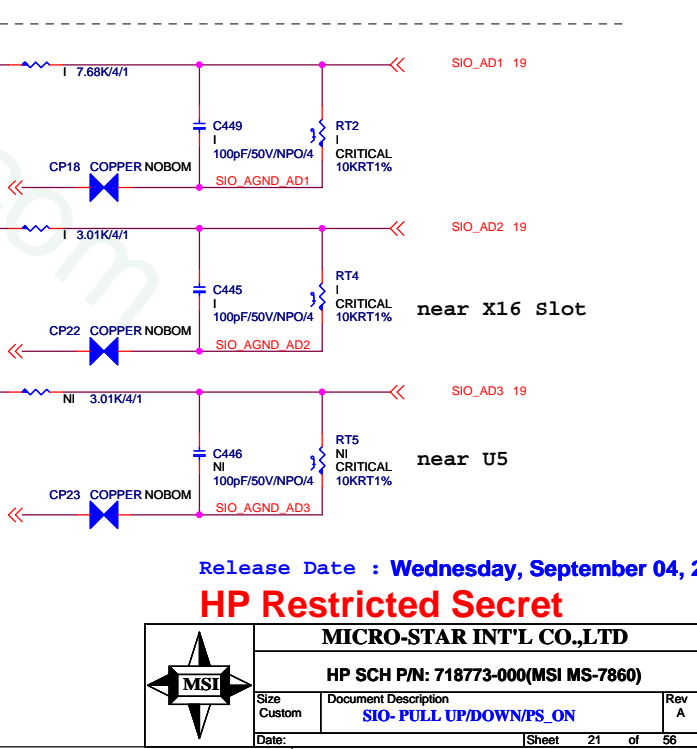
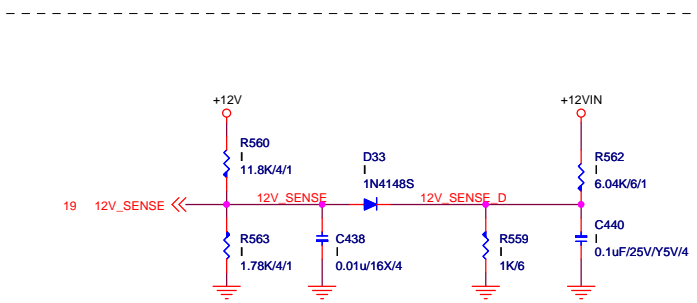
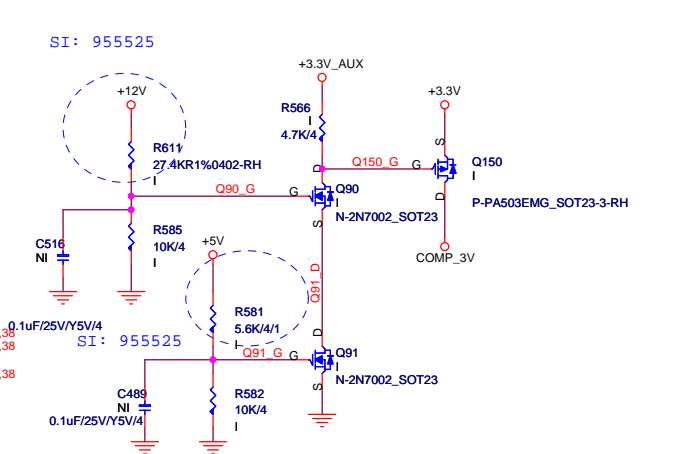
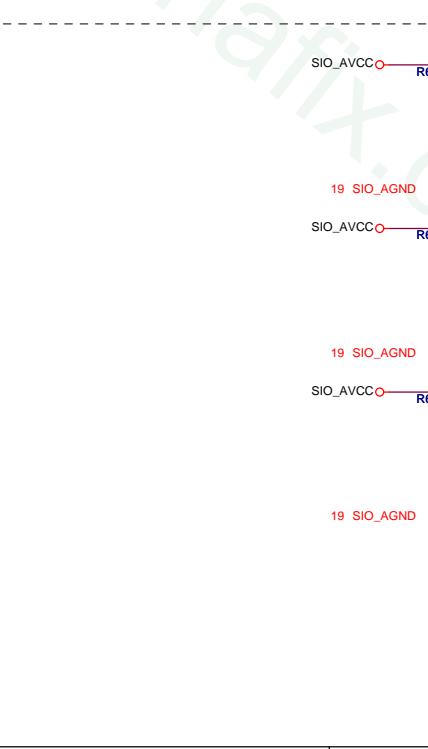
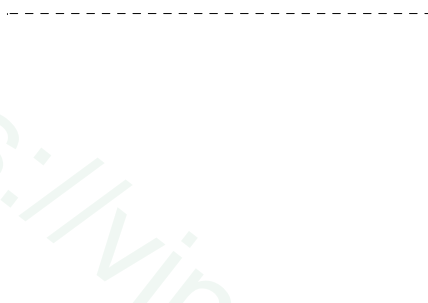
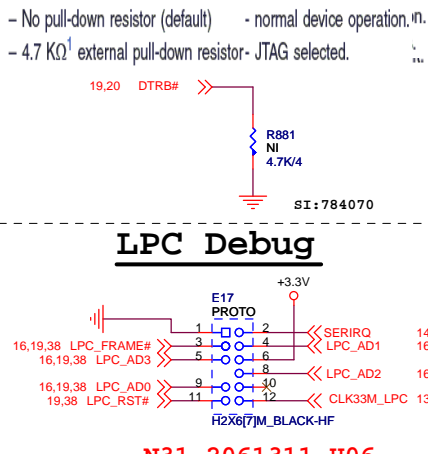
KB / MS / COM / LPT

Rev A

SYSOPT Strap (RTS1-):
R124 - 0x2E* DEFAULT
R144 - 0x4E



- 10 K Ω external pull-up resistor - Workstations pins default.
- 10 K Ω external pull-down resistor - Desktop pins default.
- No pull-down resistor (default) - normal device operation.n.
- 4.7 K Ω external pull-down resistor- JTAG selected.

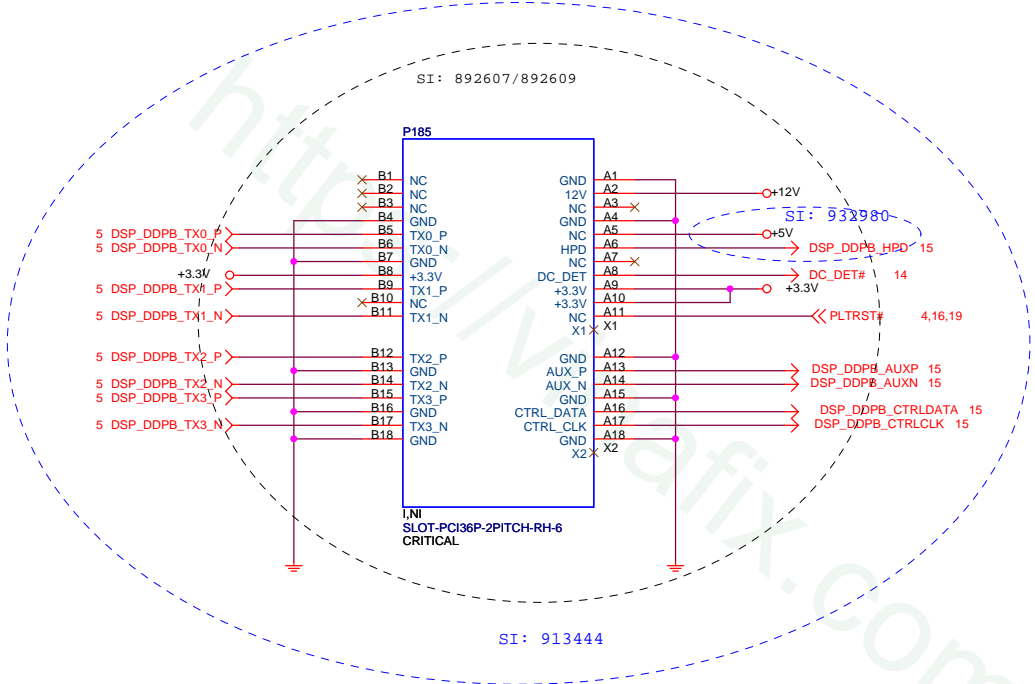


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HP SCH P/N: 718773-000(MSI MS-7860)		
Size Custom	Document Description	Rev A
SIO- PULL UP/DOWN/PS_ON		
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DDI Port Slot



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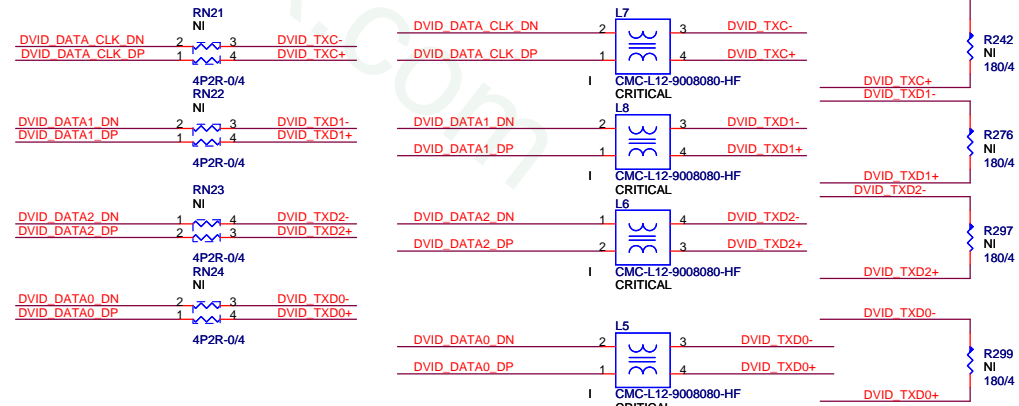
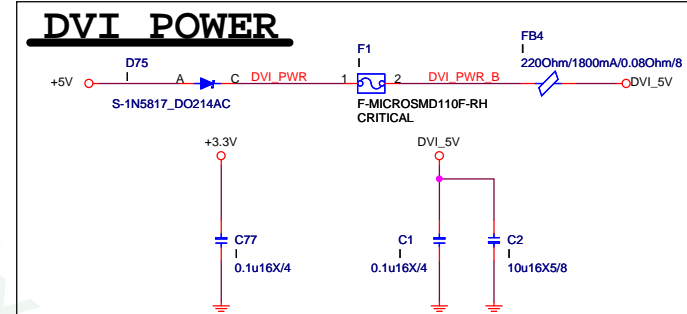
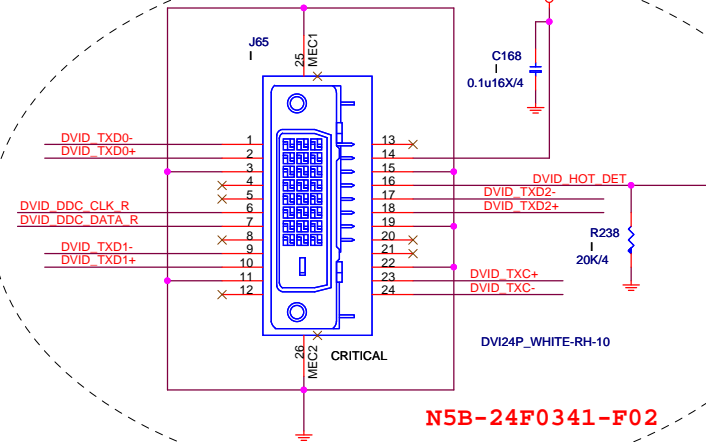
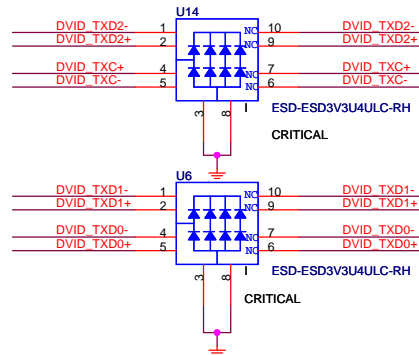
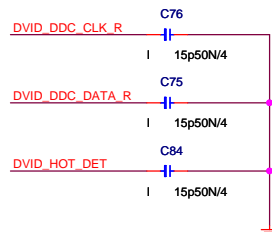
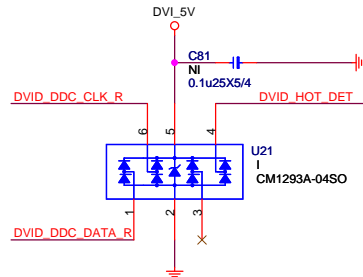
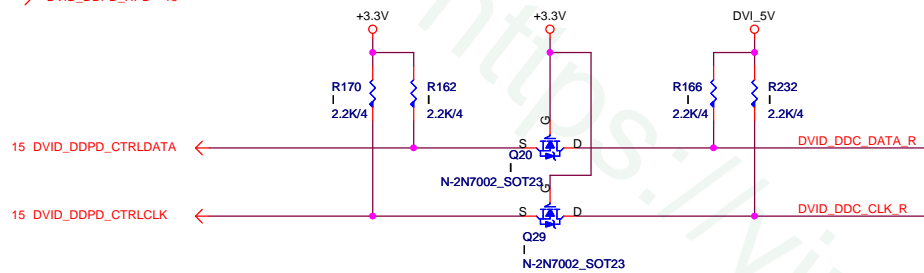
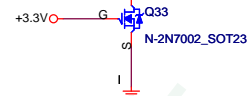
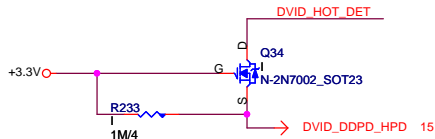
	MICRO-STAR INT'L CO.,LTD		
	HP SCH P/N: 718773-000(MSI MS-7860)		
	Size Custom	Document Description DDI Port Slot	Rev A
	Date:		Sheet 22 of 56

DVID level shifter

SI: 892611/892614

5 DVID_DDPD_CLK_P C66 0.1u16X/4 DVID_DATA_CLK_DP
5 DVID_DDPD_CLK_N C69 0.1u16X/4 DVID_DATA_CLK_DN
5 DVID_DDPD_TX2_P C56 0.1u16X/4 DVID_DATA2_DP
5 DVID_DDPD_TX2_N C57 0.1u16X/4 DVID_DATA2_DN
5 DVID_DDPD_TX1_P C58 0.1u16X/4 DVID_DATA1_DP
5 DVID_DDPD_TX1_N C61 0.1u16X/4 DVID_DATA1_DN
5 DVID_DDPD_TX0_P C51 0.1u16X/4 DVID_DATA0_DP
5 DVID_DDPD_TX0_N C53 0.1u16X/4 DVID_DATA0_DN

Q33 D R181 680/4 DVID_DATA_CLK_DN
R164 680/4 DVID_DATA_CLK_DP
R173 680/4 DVID_DATA1_DN
R138 680/4 DVID_DATA1_DP
R140 680/4 DVID_DATA2_DN
R172 680/4 DVID_DATA2_DP
R103 680/4 DVID_DATA0_DN
R112 680/4 DVID_DATA0_DP

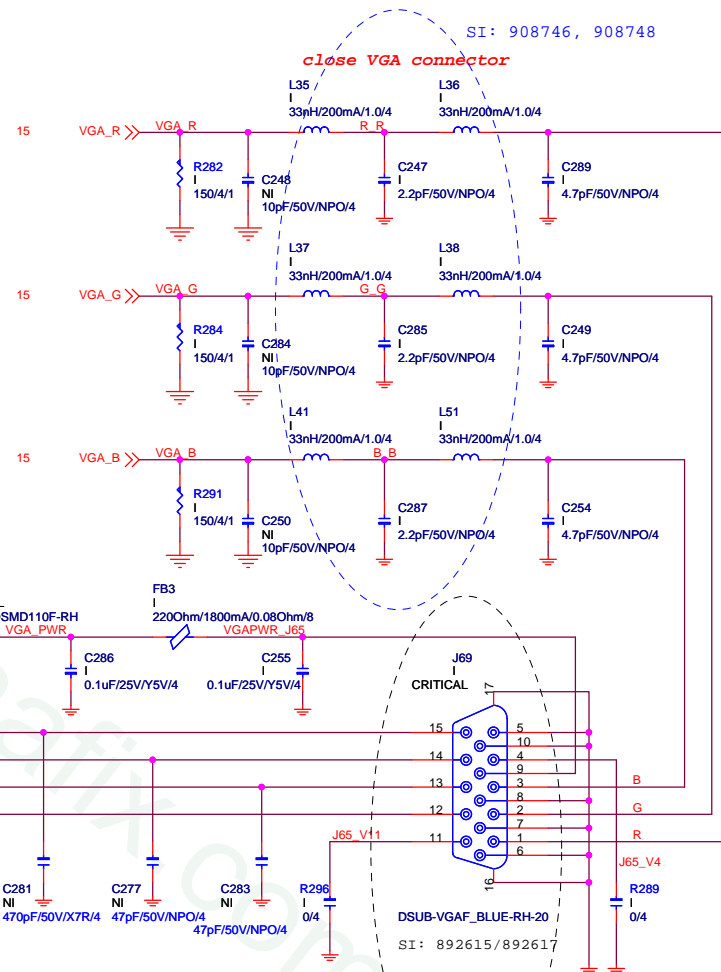
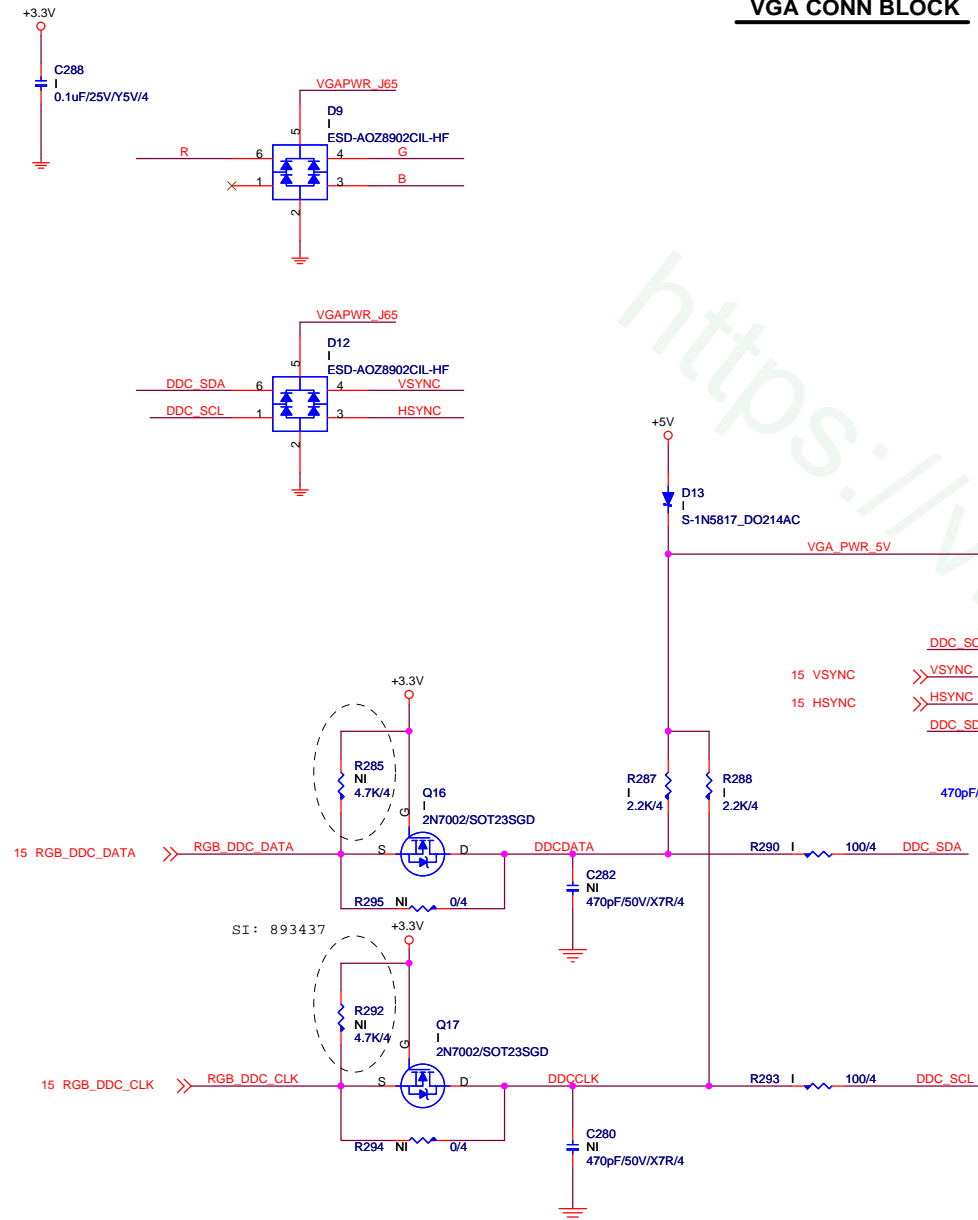


Release Date : Wednesday, September 04, 2013

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HP SCH P/N: 718773-000(MSI MS-7860)		
Size Custom	Document Description DVI Port CONN	Rev A
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VGA CONN BLOCK



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HP SCH P/N: 718773-000(MSI MS-7860)

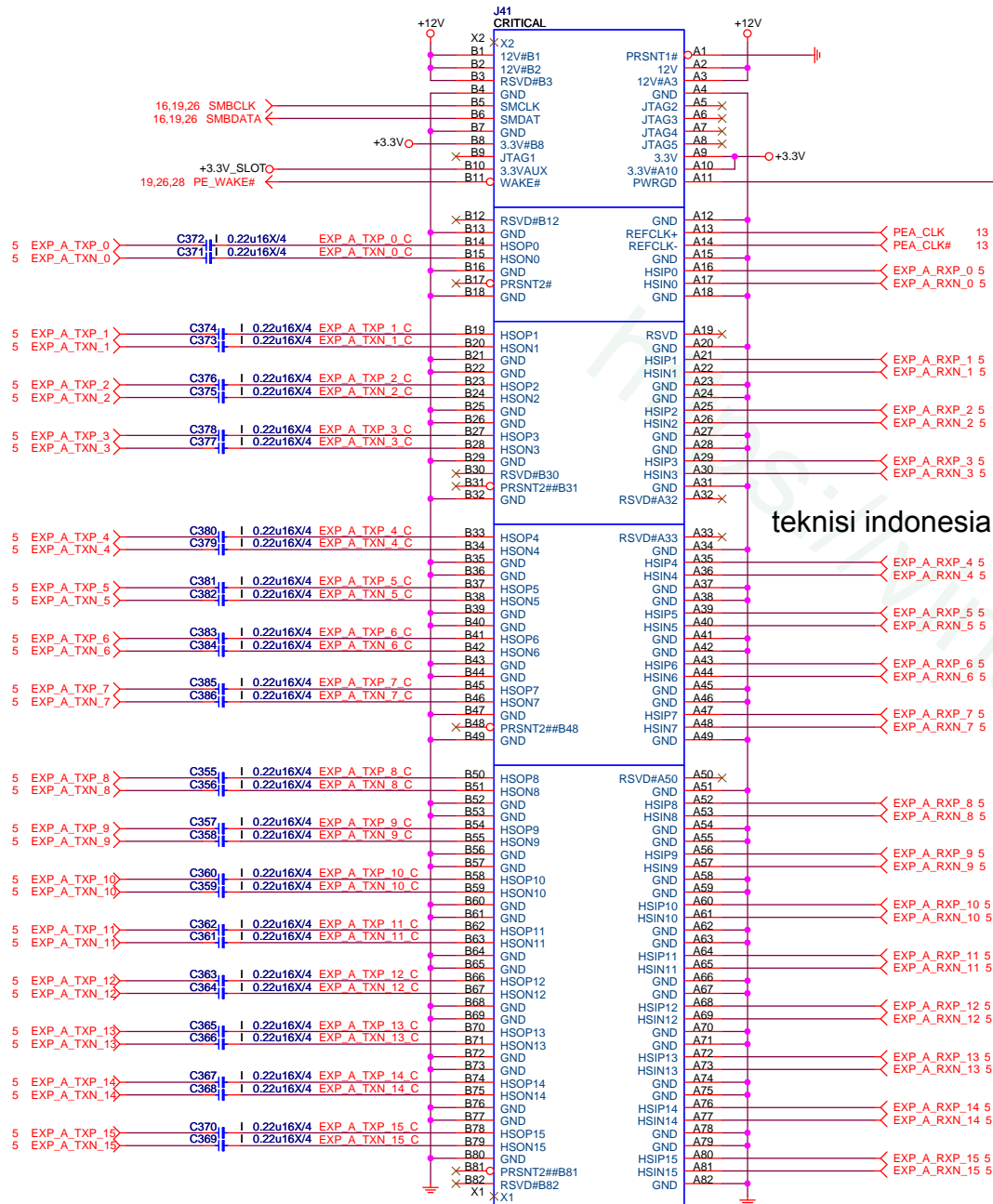
Document Description
VGA CONN

Date:

Rev
A

Sheet 24 of 56

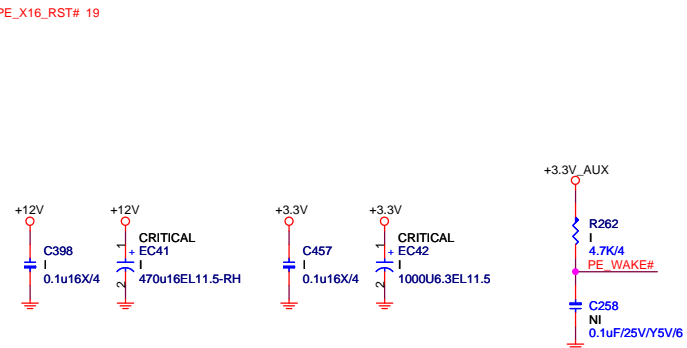
PCI EXPRESS X16 SLOT



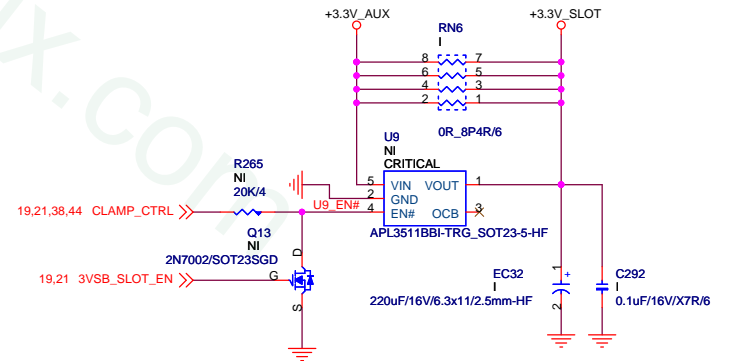
SLOT-PCI164P_BLACK-2PITCH-RH-20

N11-1641151-L06

teknisi indonesia



+3.3V SLOT



Release Date : Wednesday, September 04, 2013

HP Restricted Secret

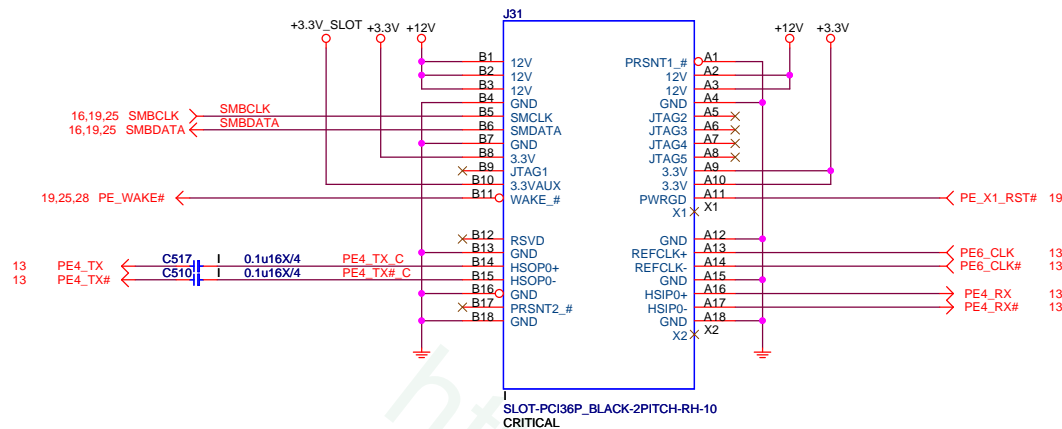


MICRO-STAR INT'L CO.,LTD

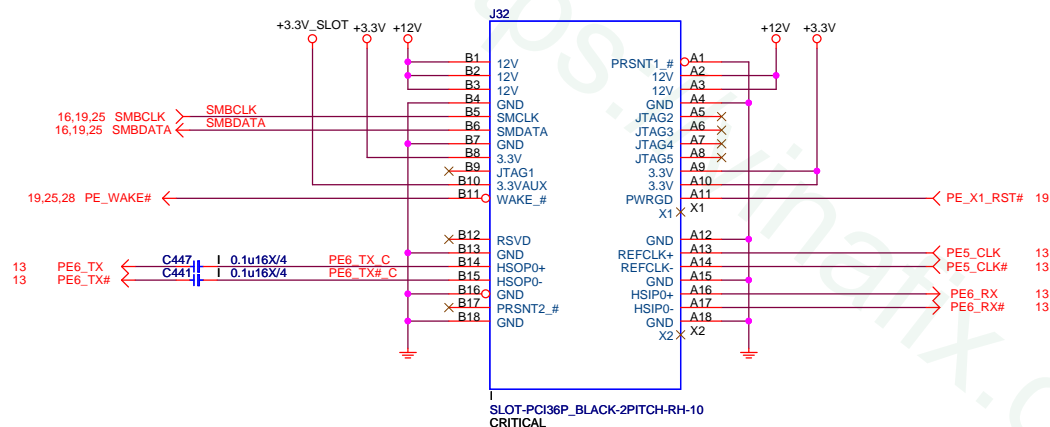
HP SCH P/N: 718773-000(MSI MS-7860)

Size	Document Description	Rev
Custom	PCIE x16 Slot	A
Date:	Sheet 25 of 56	

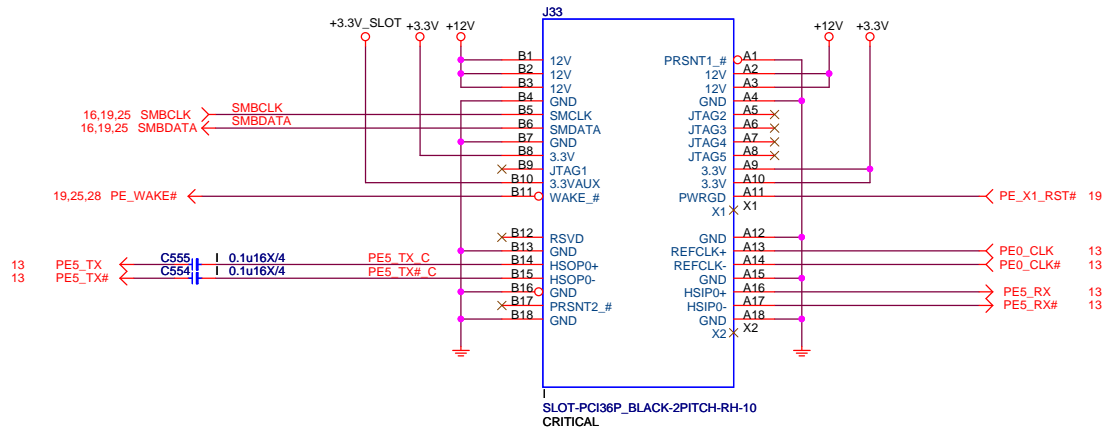
PCI EXPRESS x1-PORT



PCI EXPRESS x1-PORT



PCI EXPRESS x1-PORT



N11-0360381-L06

Release Date : Wednesday, September 04, 2013

HP Restricted Secret

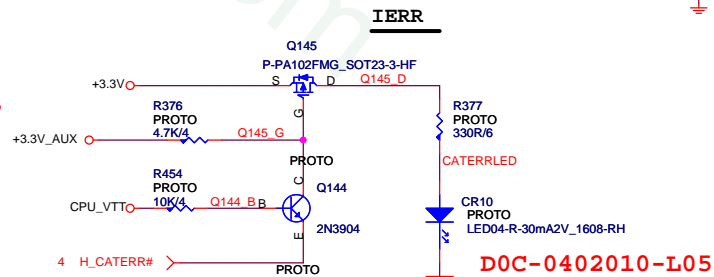
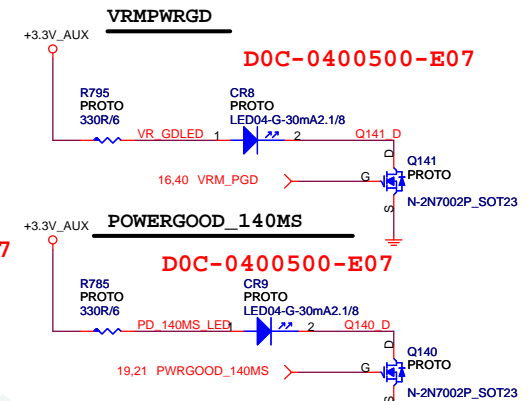
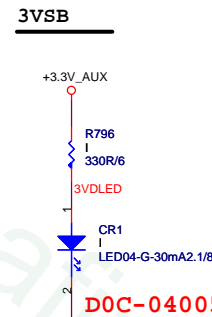
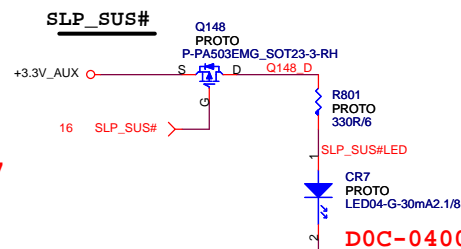
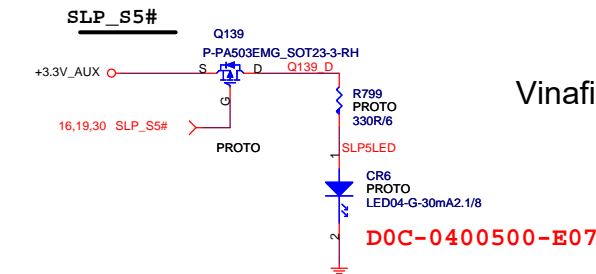
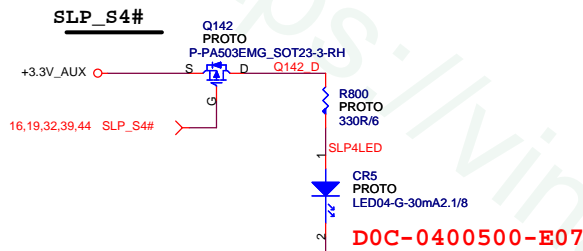
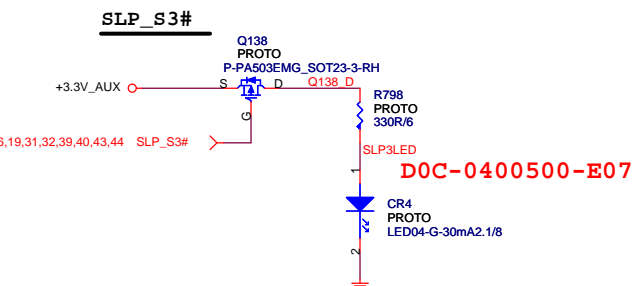
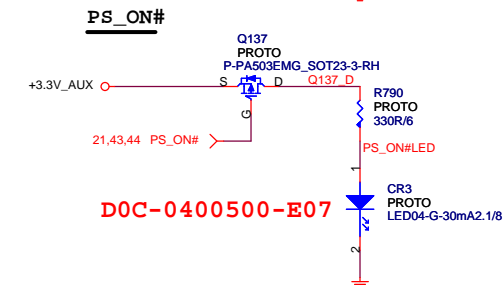
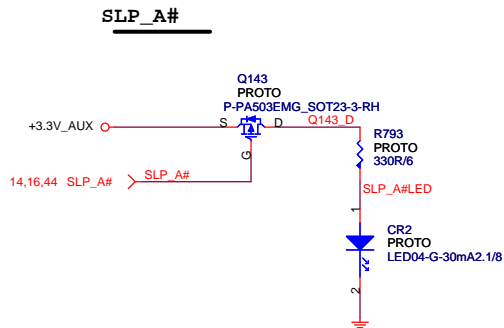
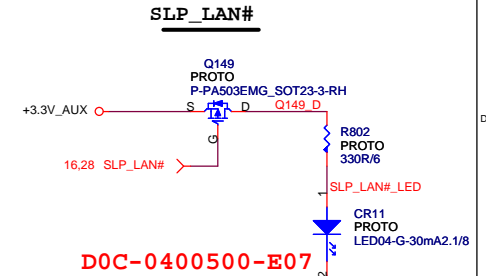
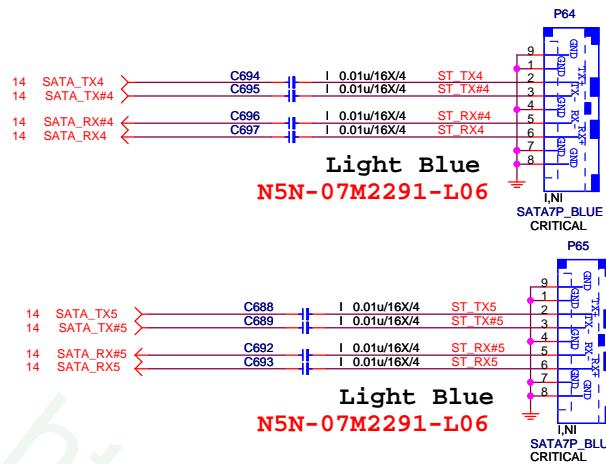
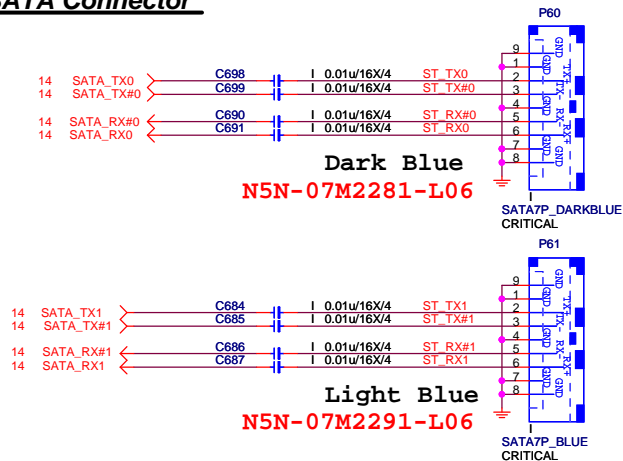


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Size	Document Description	Rev
Custom	PCIE x1 Slots	A
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SATA Connector

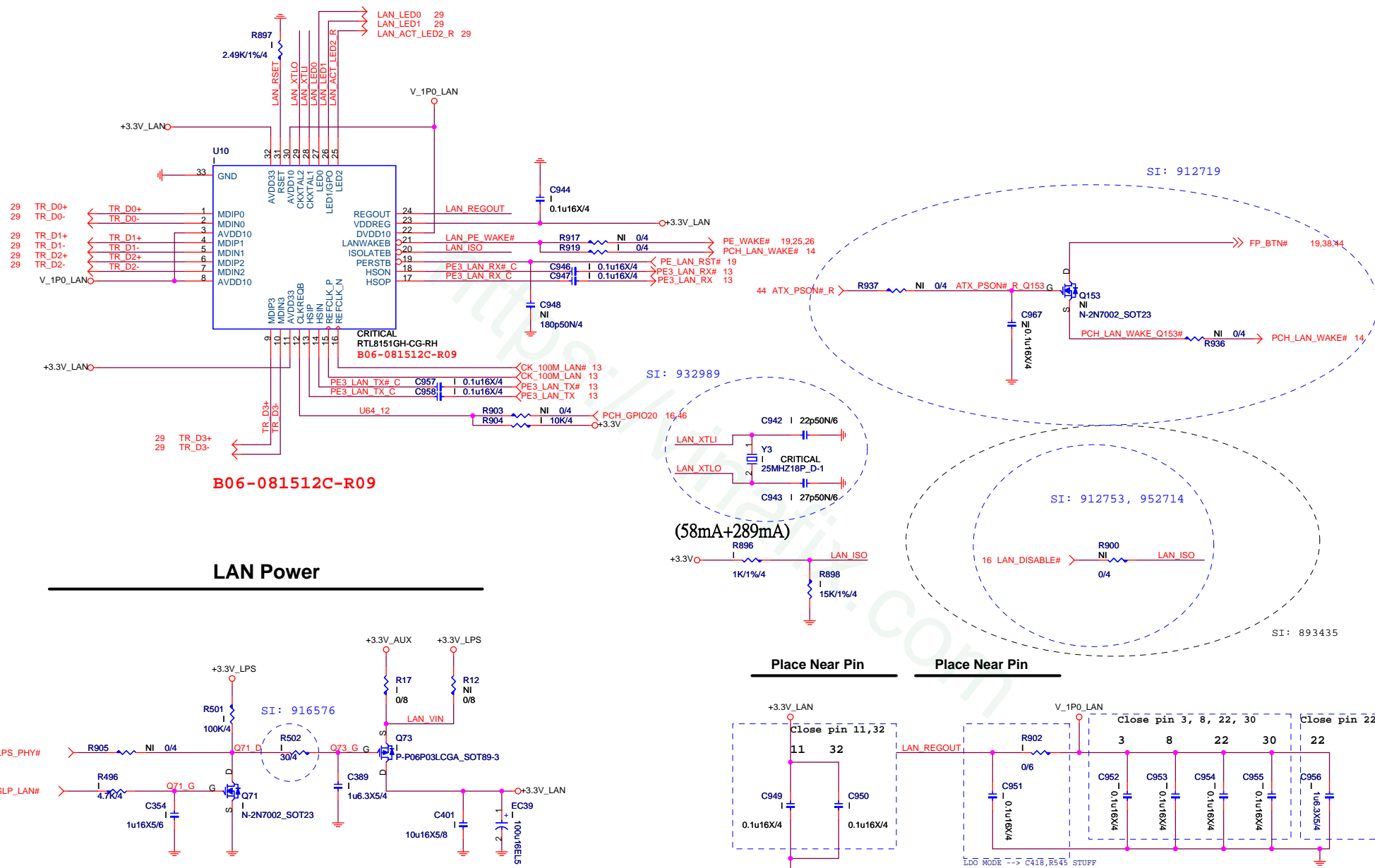


Release Date : Wednesday, September 04, 2013

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			MICRO-STAR INT'L CO.,LTD	
			HP SCH P/N: 718773-000(MSI MS-7860)	
Size Custom	Document Description SATA/LED		Rev A	
Date:			Sheet 27	of 56

Gigabit LAN RTL8151GH-CG



Release Date : Wednesday, September 04, 2013

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MICRO-STAR INT'L CO.,LTD

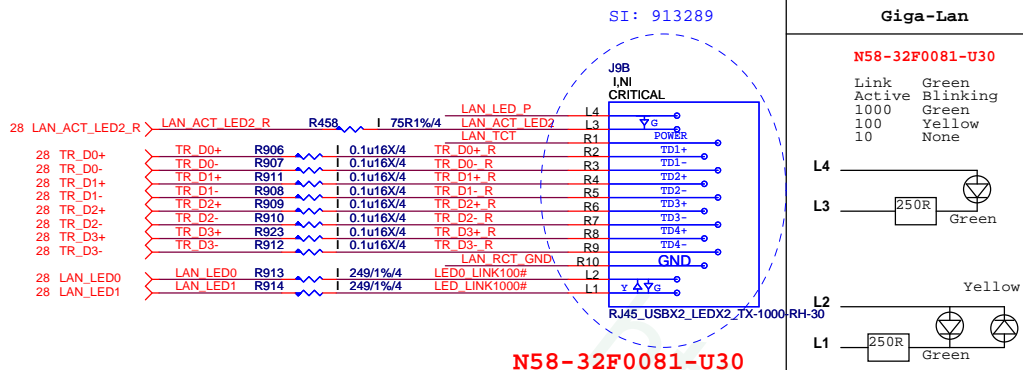
HP SCH P/N: 718773-000(MSI MS-7860)

n	Document Description
	Gigabit LAN-RTL8151GH-CG

Date:	Sheet 28 of 56
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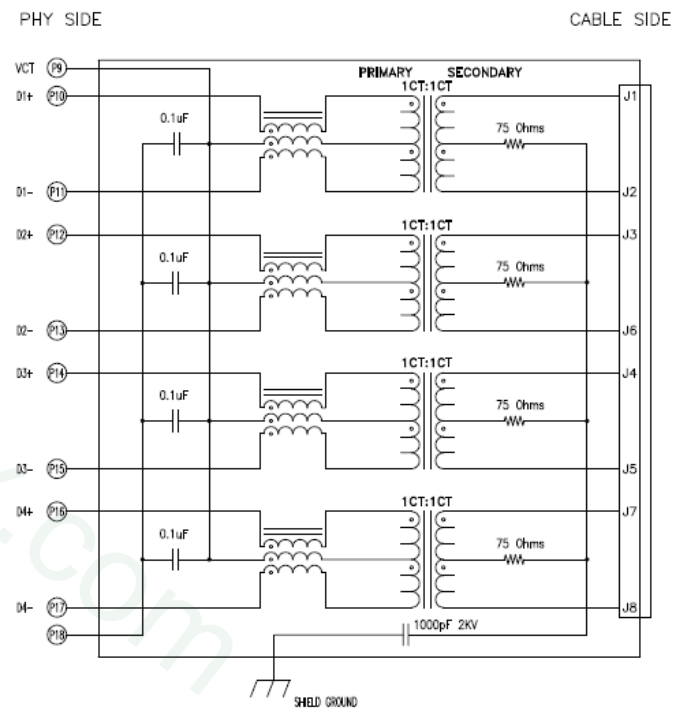


LAN Connector

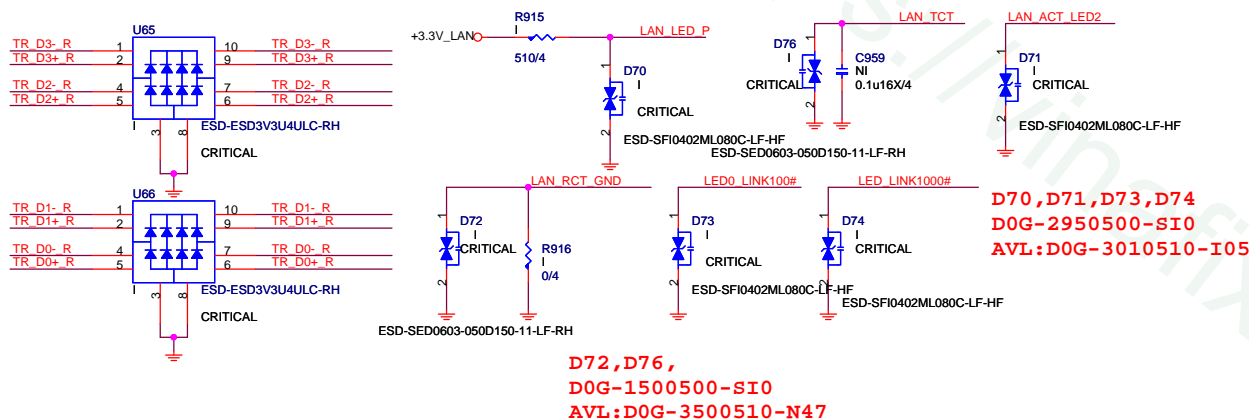


Function	Link LED	Speed LED
10Mb Link	Green (solid)	Off
100Mb Link	Green (solid)	Yellow (solid)
1000Mb Link	Green (solid)	Green (solid)
10Mb Data Transfer	Green (blink)	Off
100Mb Data Transfer	Green (blink)	Yellow (solid)
1000Mb Data Transfer	Green (blink)	Green (solid)

SCHEMATIC



ESD



Release Date : Wednesday, September 04, 2013

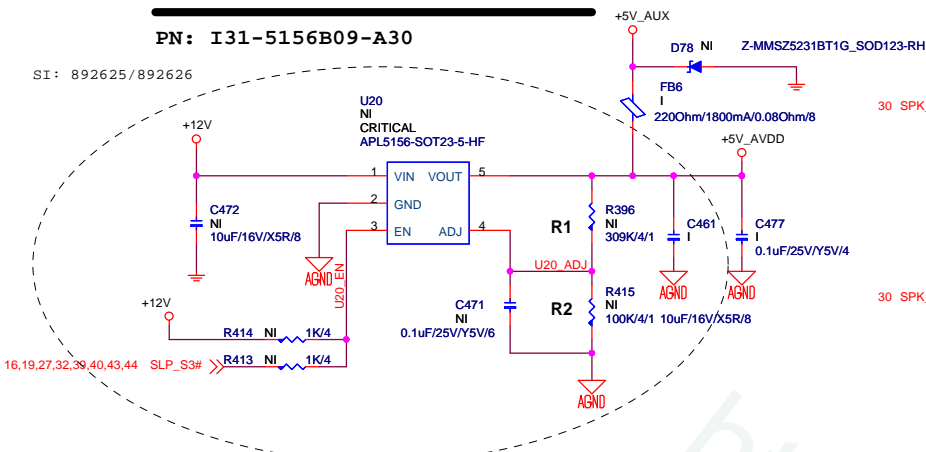
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HP SCH P/N: 718773-000(MSI MS-7860)		
Size Custom	Document Description LAN CONNECTOR	Rev A
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AUDIO CODEC REGULATORS

PN: I31-5156B09-A30

SI: 892625/892626



SPEAKER HEADER

P/N:N32-1020521-H06

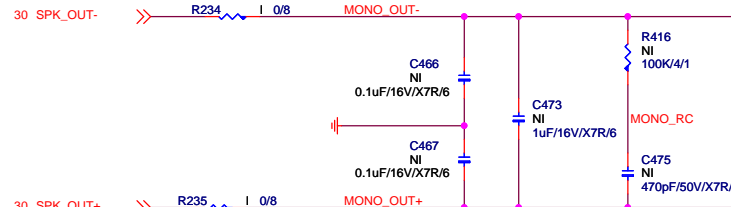


TABLE 14
SPEAKER HEADER DEFINITION

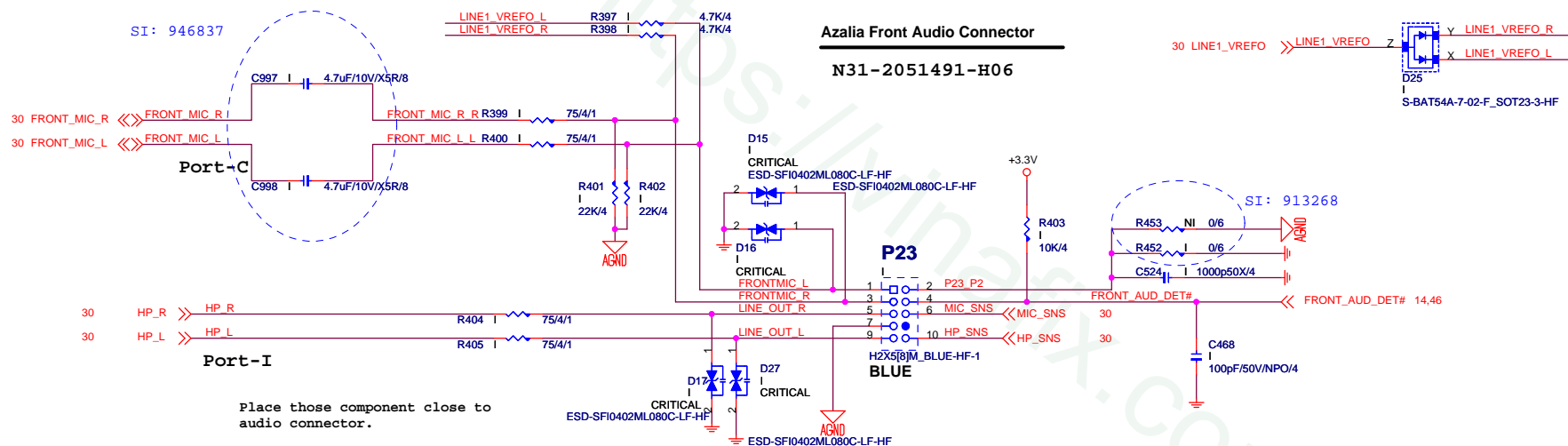
P6	
SPEAKER-	1
SPEAKER+	2

SPK+- TRACE WIDTH

Speaker 4 ohm ==> 40mils

Speaker 8 ohm ==> 20mils

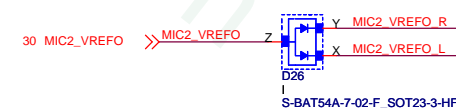
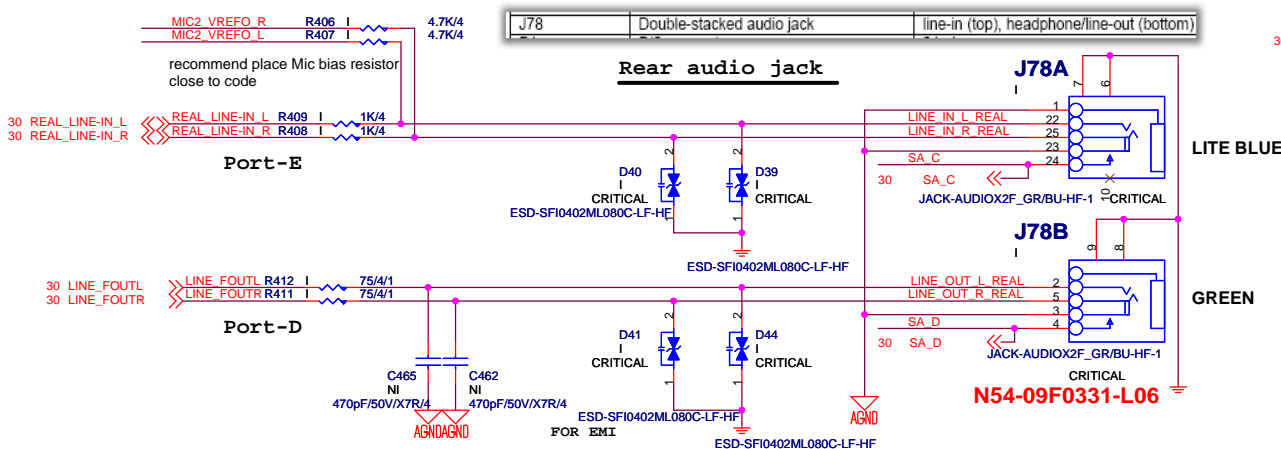
SI: 946837



Place those component close to audio connector.

Rear audio jack

J78 Double-stacked audio jack line-in (top), headphone/line-out (bottom)



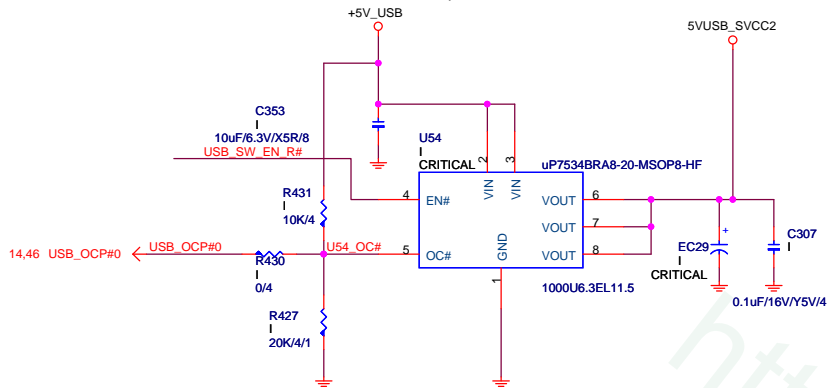
D15, D16, D17, D27, D39, D40, D41, D44
D0G-2950500-SI0
AVL:D0G-3010510-I05

Release Date : Wednesday, September 04, 2013

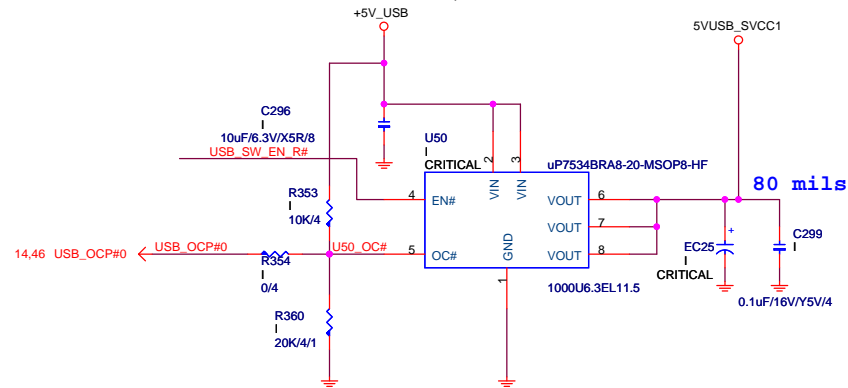
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MICRO-STAR INT'L CO.,LTD		
HP SCH P/N: 718773-000(MSI MS-7860)		
Size Custom	Document Description	Rev A
AUDIO CONNECTOR		
Date:	Sheet 31	of 56

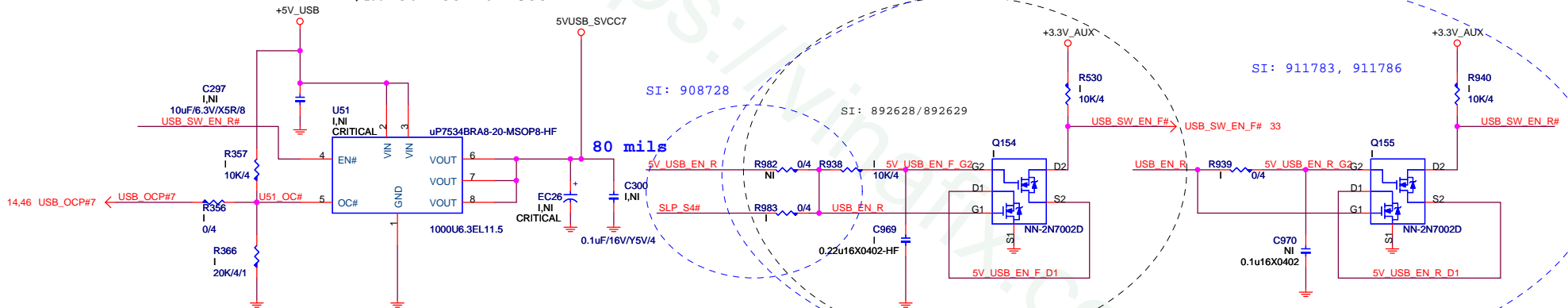
POWER CIRCUIT FOR USB PORT 2,3 P/N: I36-7534B02-U33



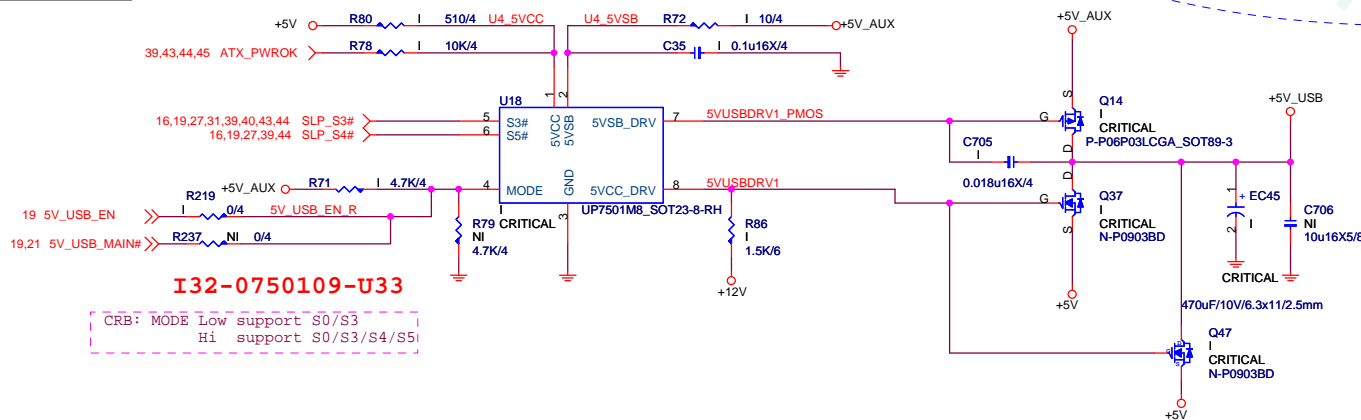
POWER CIRCUIT FOR USB PORT 0,1 P/N: I36-7534B02-U33



POWER CIRCUIT FOR USB PORT 12,13 P/N: I36-7534B02-U33



USB POWER



I32-0750109-U33

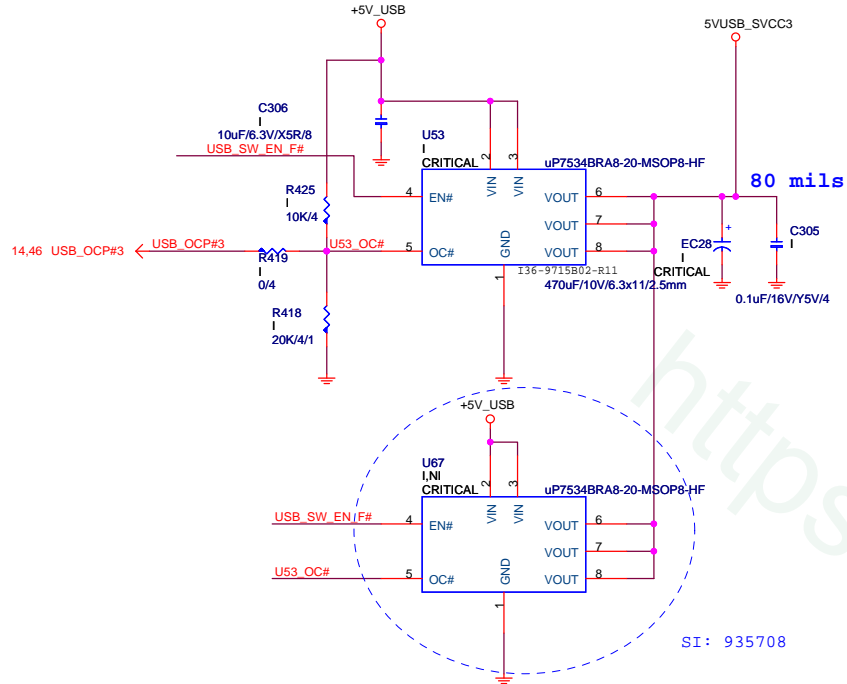
CRB: MODE Low support S0/S3
Hi support S0/S3/S4/S5

Release Date : Wednesday, September 04, 2013

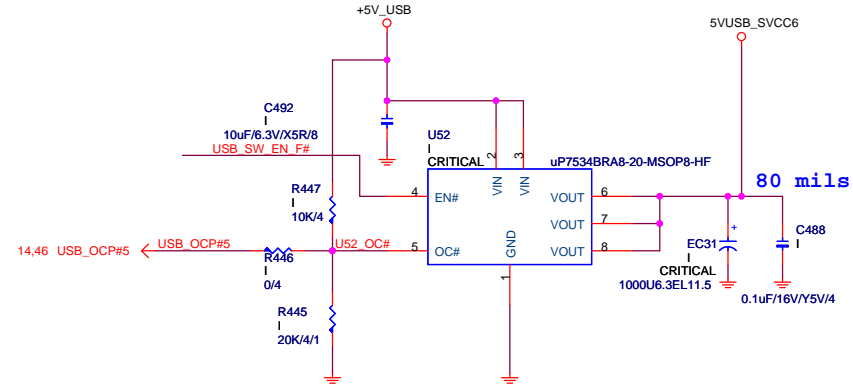
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MICRO-STAR INT'L CO.,LTD		
HP SCH P/N: 718773-000(MSI MS-7860)		
Size Custom	Document Description	Rev A
Rear USB POWER		
Date:	Sheet 32 of 56	

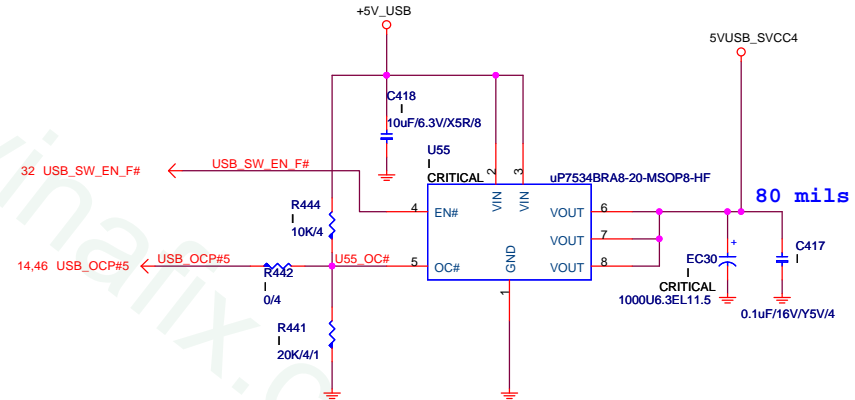
POWER CIRCUIT FOR USB PORT 4,5,6 P/N: I36-7534B02-U33



POWER CIRCUIT FOR USB PORT 10,11 P/N: I36-7534B02-U33




POWER CIRCUIT FOR USB PORT 8,9 P/N: I36-7534B02-U33



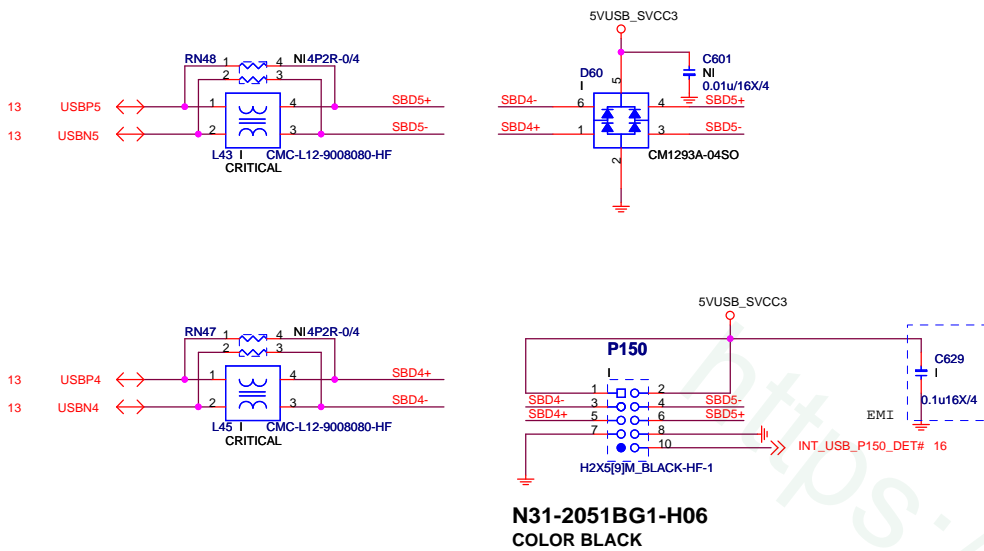
Vinafix.com

Release Date : Wednesday, September 04, 2013

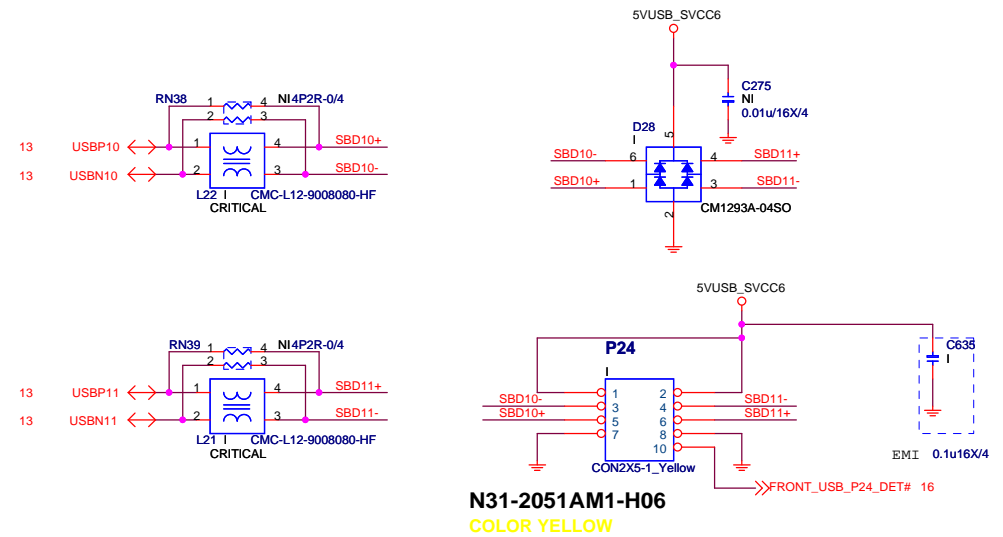
HP Restricted Secret

			MICRO-STAR INT'L CO.,LTD	
HP SCH P/N: 718773-000(MSI MS-7860)		Document Description		Rev A
Date:		Sheet 33 of 56		

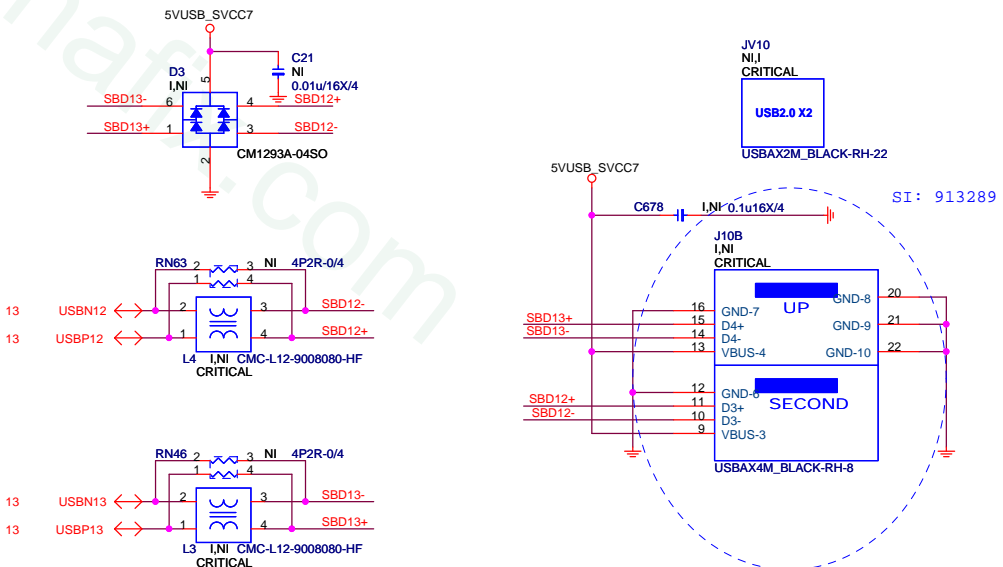
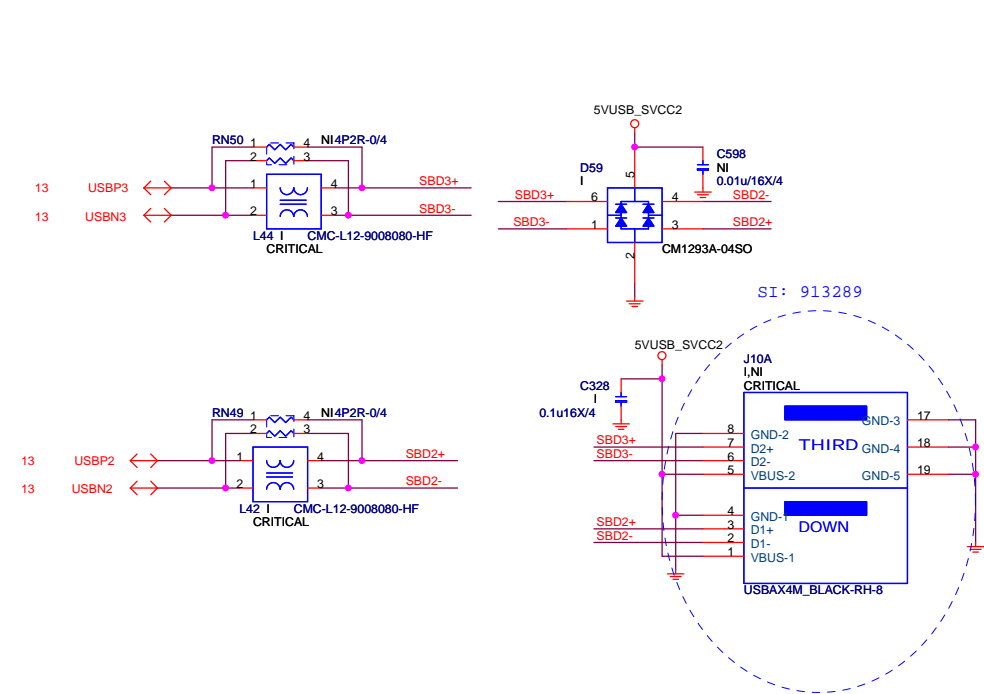
Internal USB Connector For USB Port 4 / 5



Front Panel USB Connector For USB Port 10 / 11



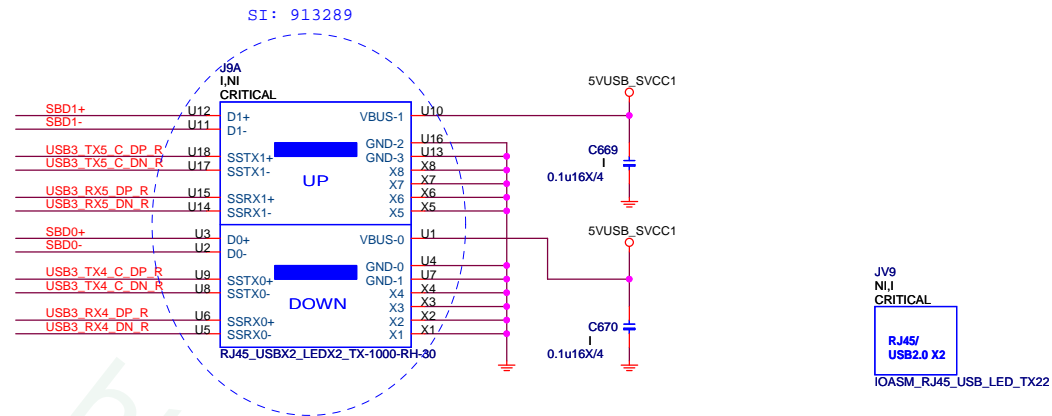
Rear USB Connector For USB Port 2/3



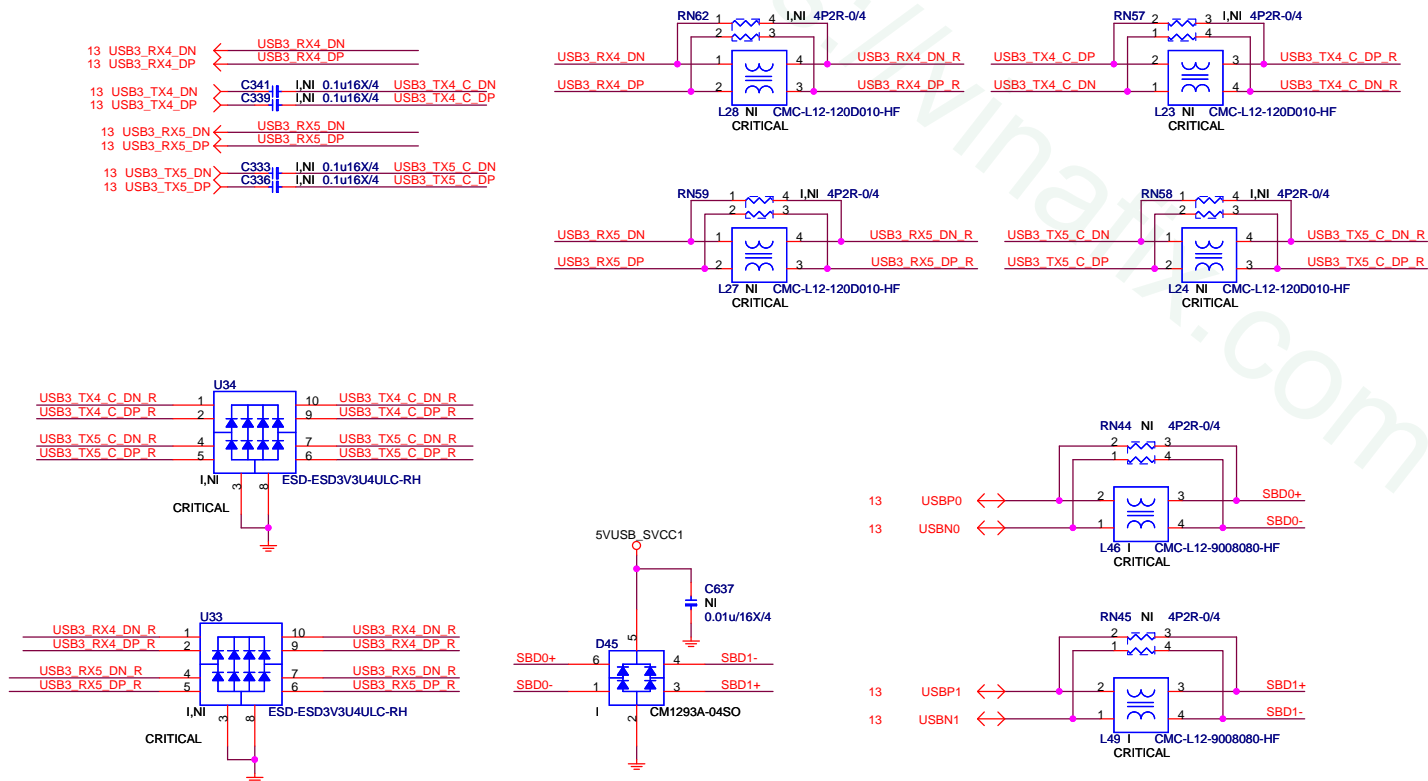
Release Date : Wednesday, September 04, 2013

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HP SCH P/N: 718773-000(MSI MS-7860)		
Size Custom	Document Description	Rev A
Date:	USB2.0	
Sheet 34 of 56		



REAR USB3.0 Connector For USB3.0 Port 4 /5

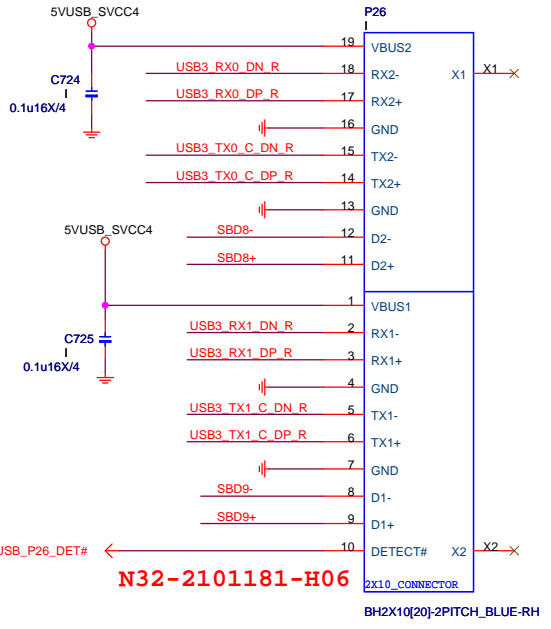
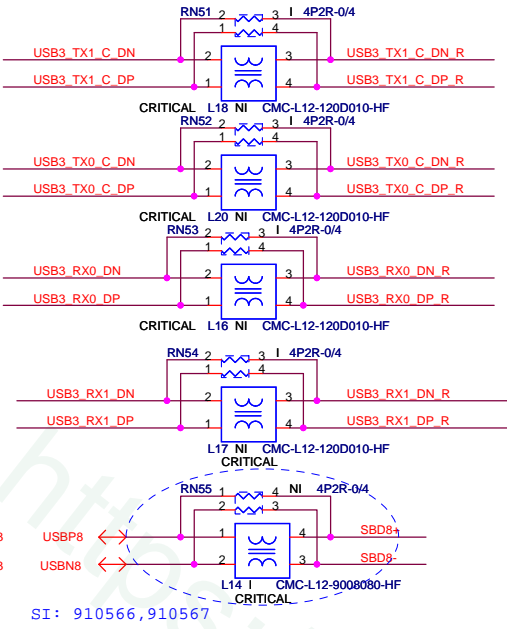
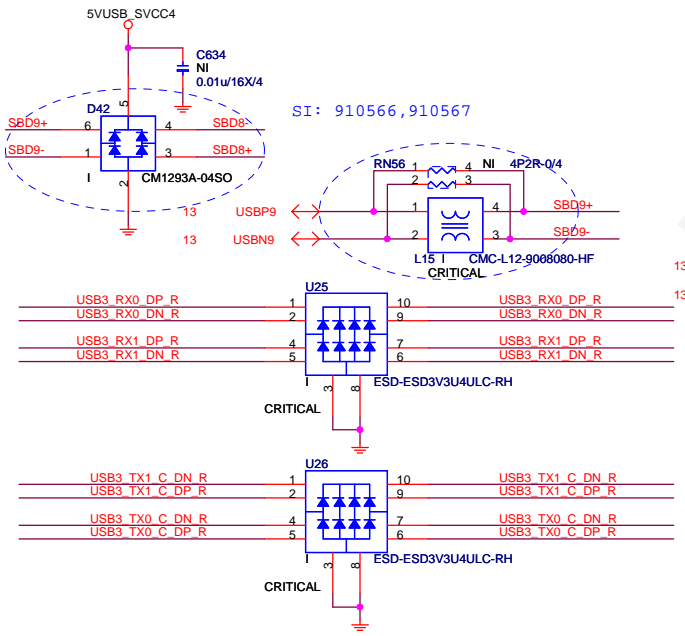
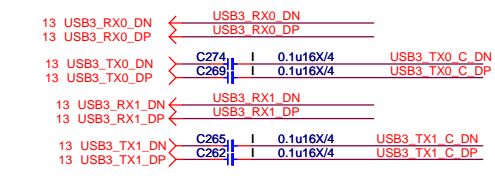


Release Date : Wednesday, September 04, 2013

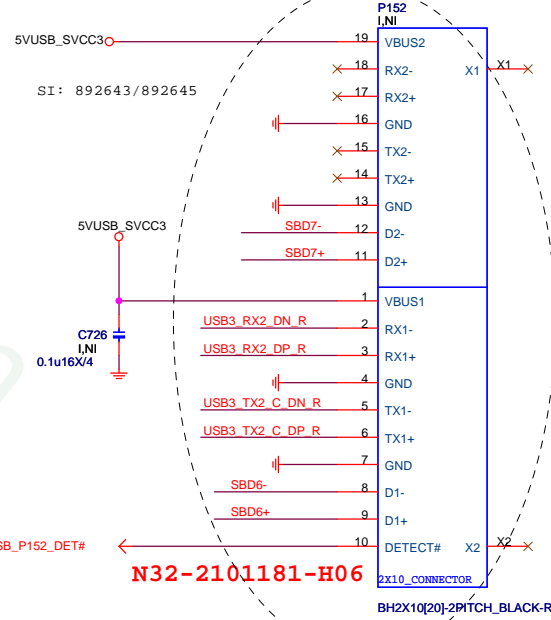
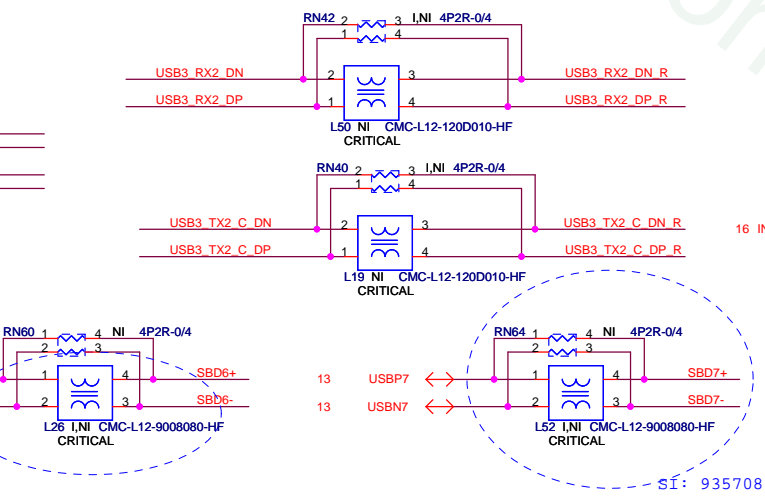
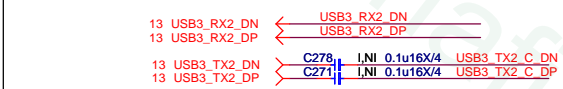
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HP SCH P/N: 718773-000(MSI MS-7860)		
Size Custom	Document Description Rear USB 3.0	Rev A
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FRONT USB3.0 Connector For USB3.0 Port 1 / 2



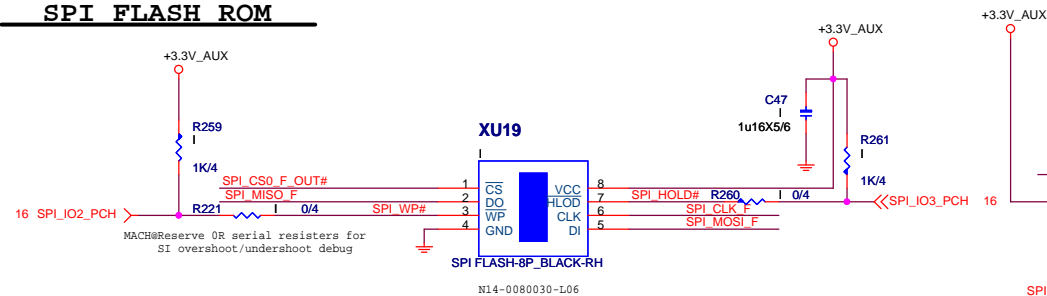
The six USB 3.0 pairs can be mapped with any USB 2.0 pair to a given connector but ACPI tables and BIOS should be updated to reflect the USB 2.0 to USB 3.0 pair mapping., DG PAGE 159



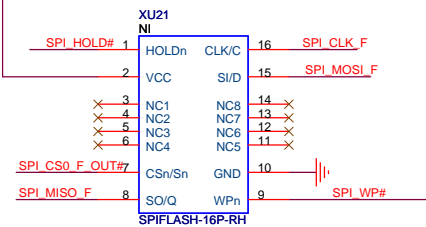
Release Date : Wednesday, September 04, 2013
HP Restricted Secret

MICRO-STAR INT'L CO.,LTD		
HP SCH P/N: 718773-000(MSI MS-7860)		
Size Custom	Document Description	Rev A
Front USB 3.0		
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SPI FLASH ROM

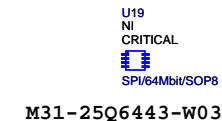


SPI 64M ROM1

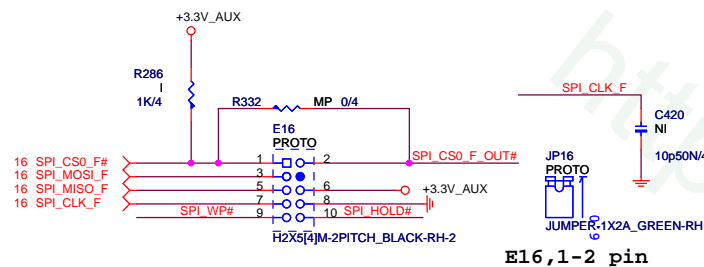


PN:N14-0160010-L06

BIOS

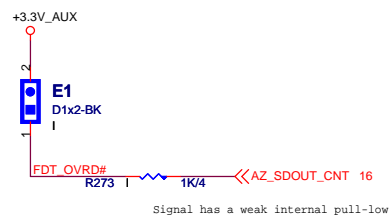


SPI DEBUG PROT



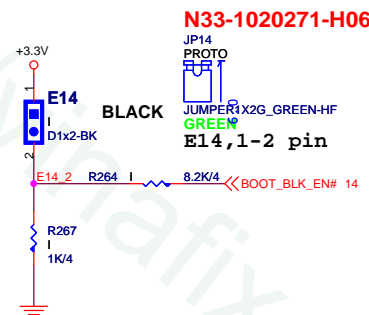
Flash Descriptor Override Header

FLASH DESCRIPTOR OVERRIDE

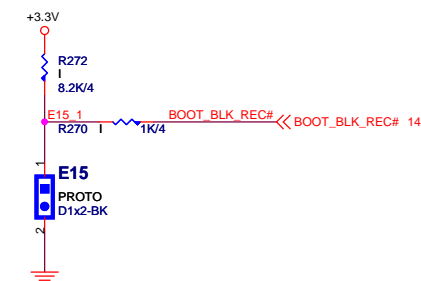


N31-1020151-H06

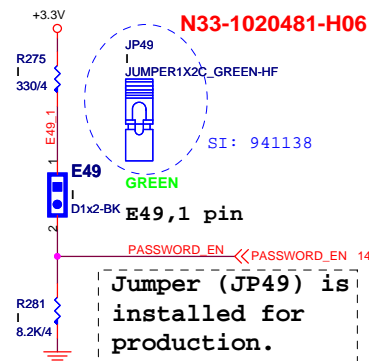
BOOT BLOCK WRITE JUMPER



BOOT BLOCK RECOVERY HEADER



PASSWORD JUMPER



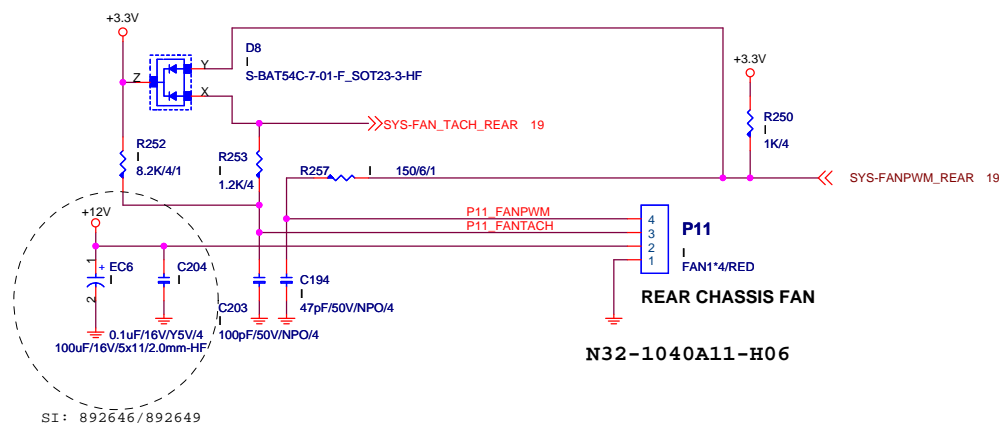
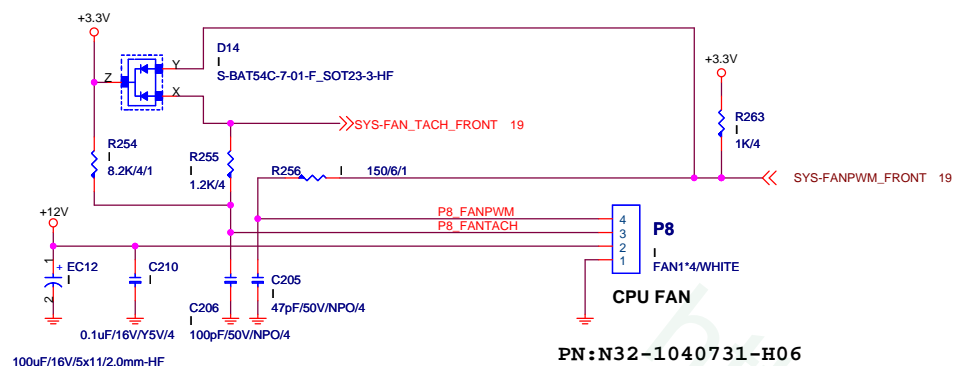
Release Date : Wednesday, September 04, 2013

HP Restricted Secret

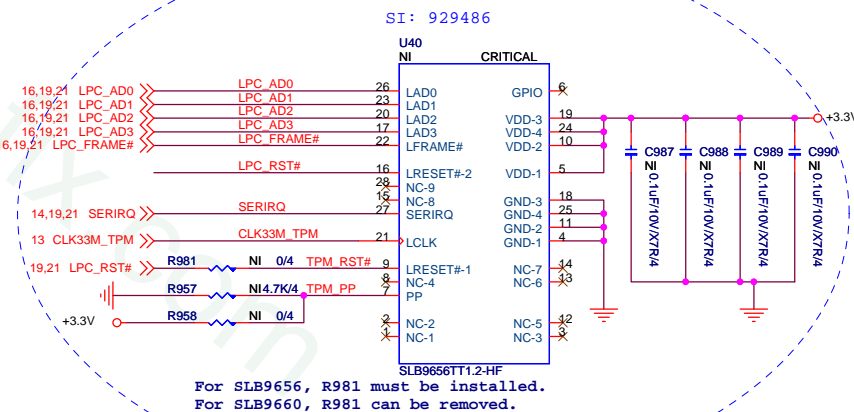
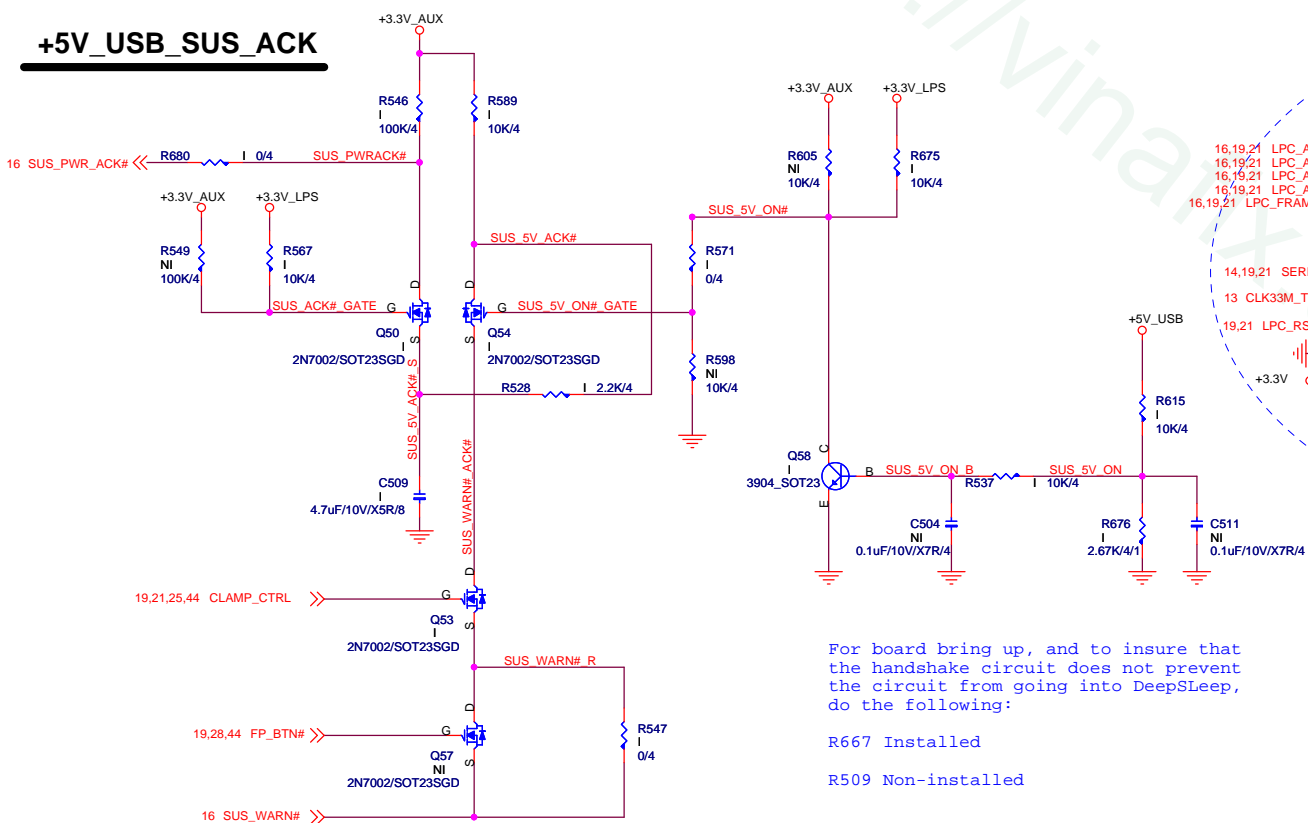


MICRO-STAR INT'L CO.,LTD			
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Size Custom	Document Description		Rev A
	Header/ SPI		
Date:		Sheet 37 of	56

FAN BLOCK



+5V_USB_SUS_ACK



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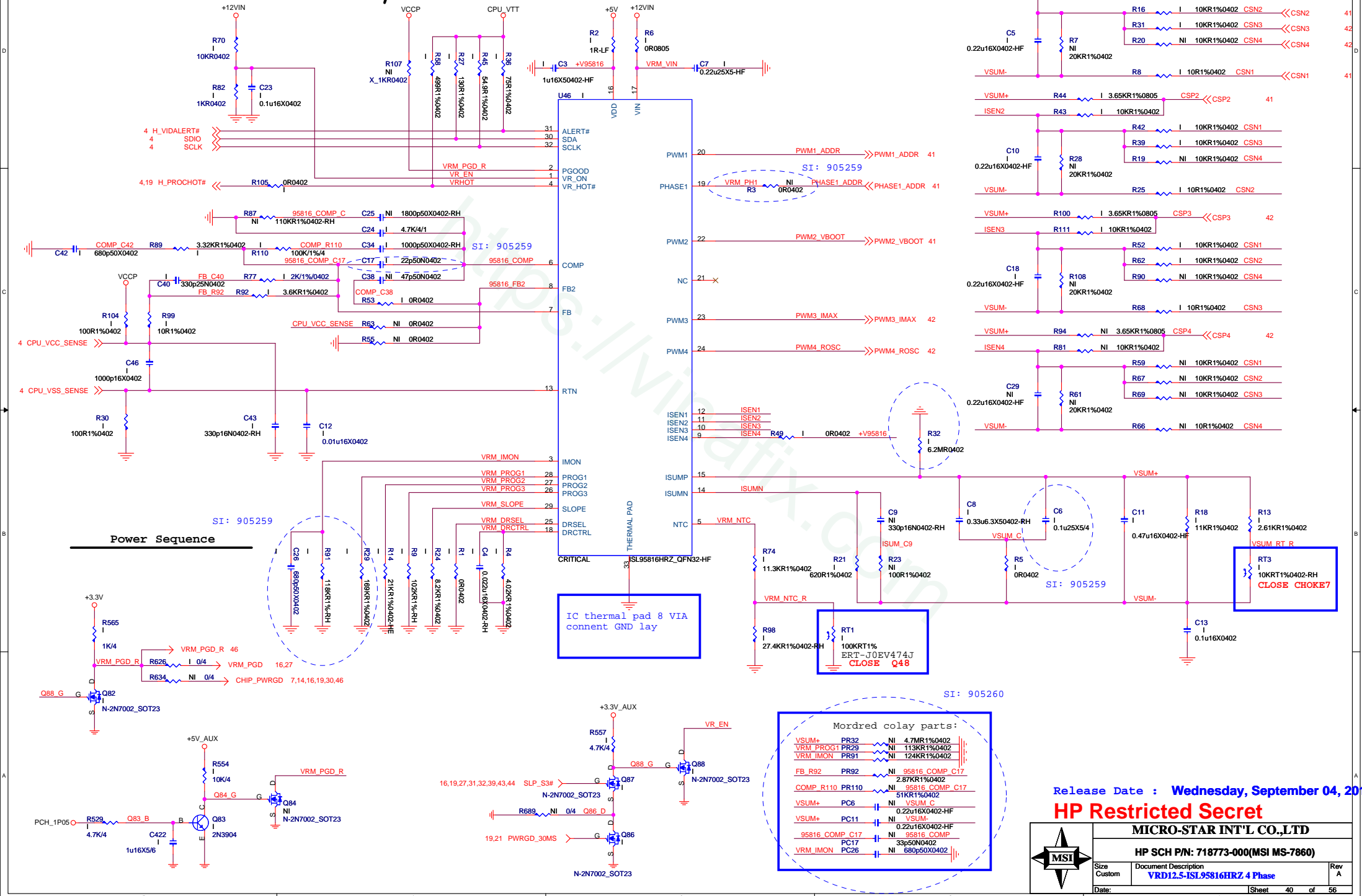
HP SCH P/N: 718773-000(MSI MS-7860)

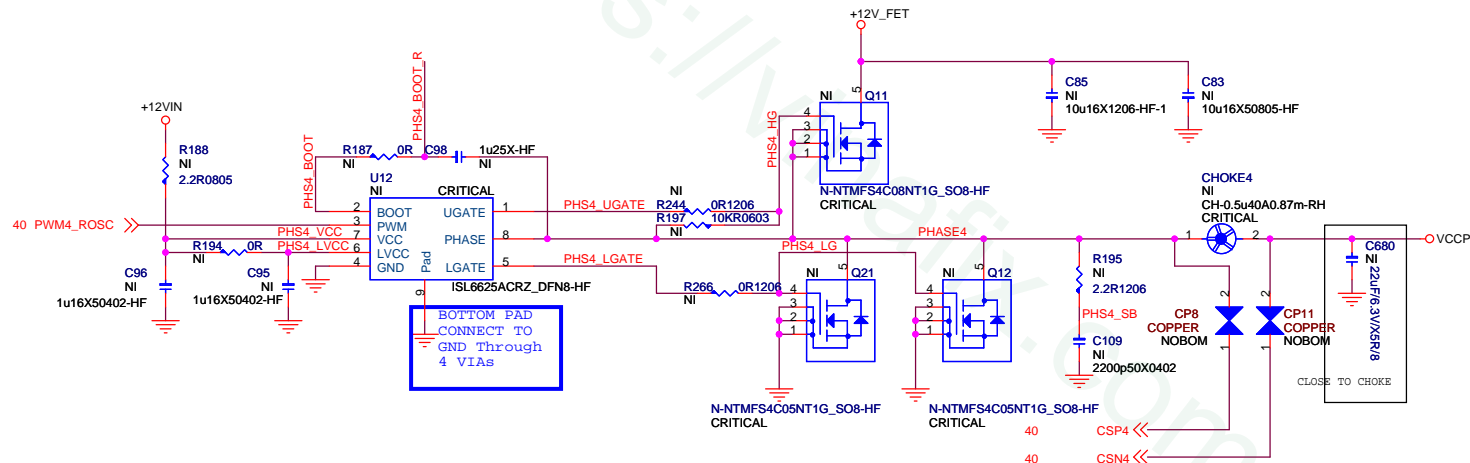
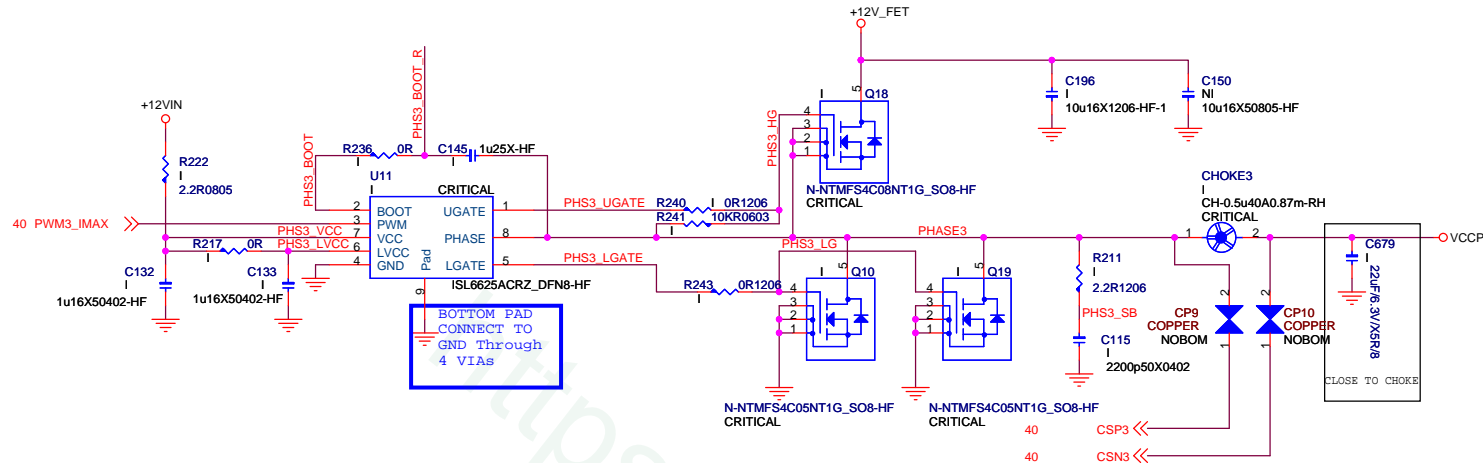
Size	Document Description
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Custom	FAN/ TPM			A
Date:		Sheet	38	of 56



SharkBay VR12.5 Power Circuit - 4 Phase





C71-5610611-N07

SI: 893441

Ceramic / 0805/X5R

Release Date : Wednesday, September 04, 2013

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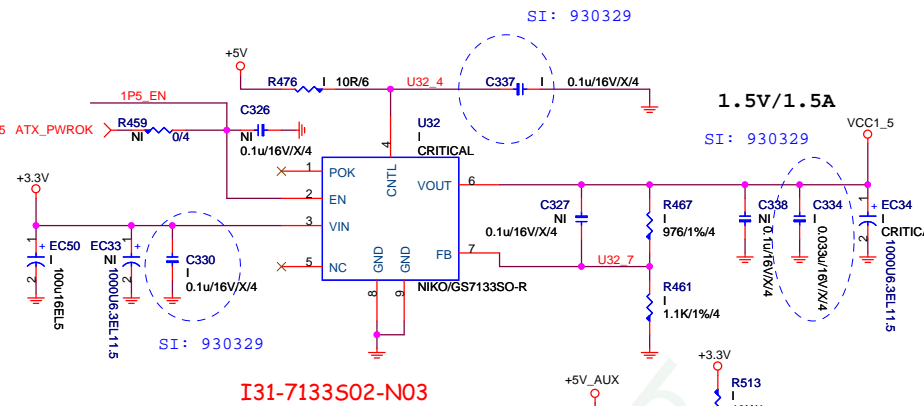


MICRO-STAR INT'L CO.,LTD

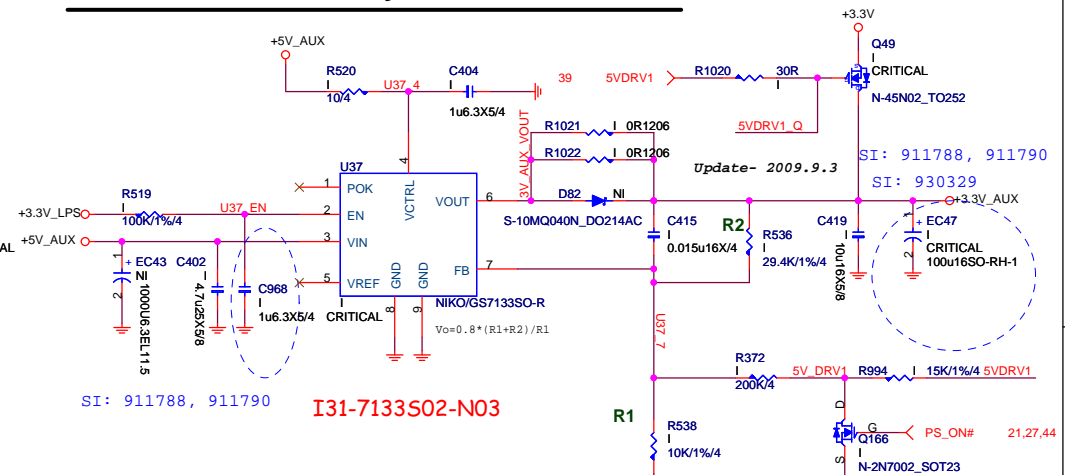
HP SCH P/N: 718773-000(MSI MS-7860)

Size Custom	Document Description VCCP-2	Rev A
Date:	Sheet 42 of 56	

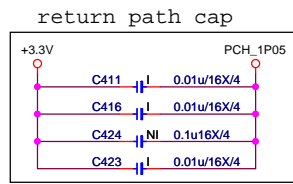
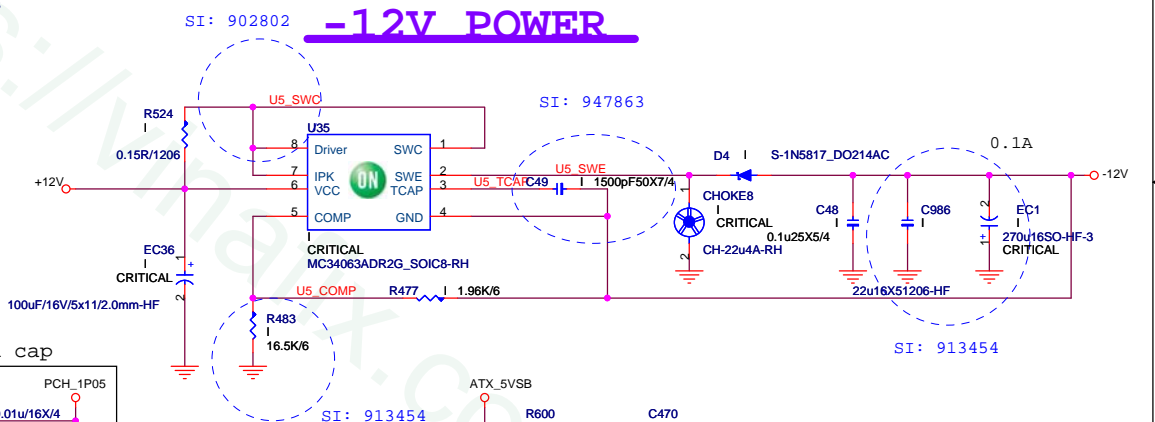
1.5V Power



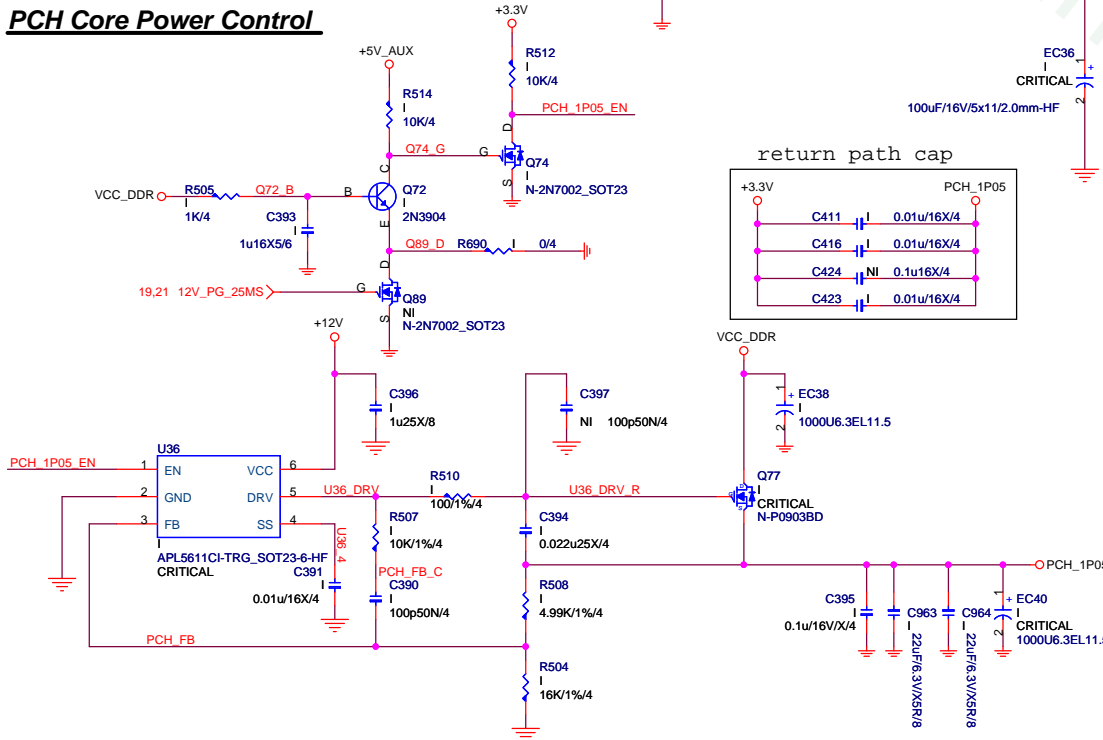
3V Standby Power



-12V POWER



PCH Core Power Control



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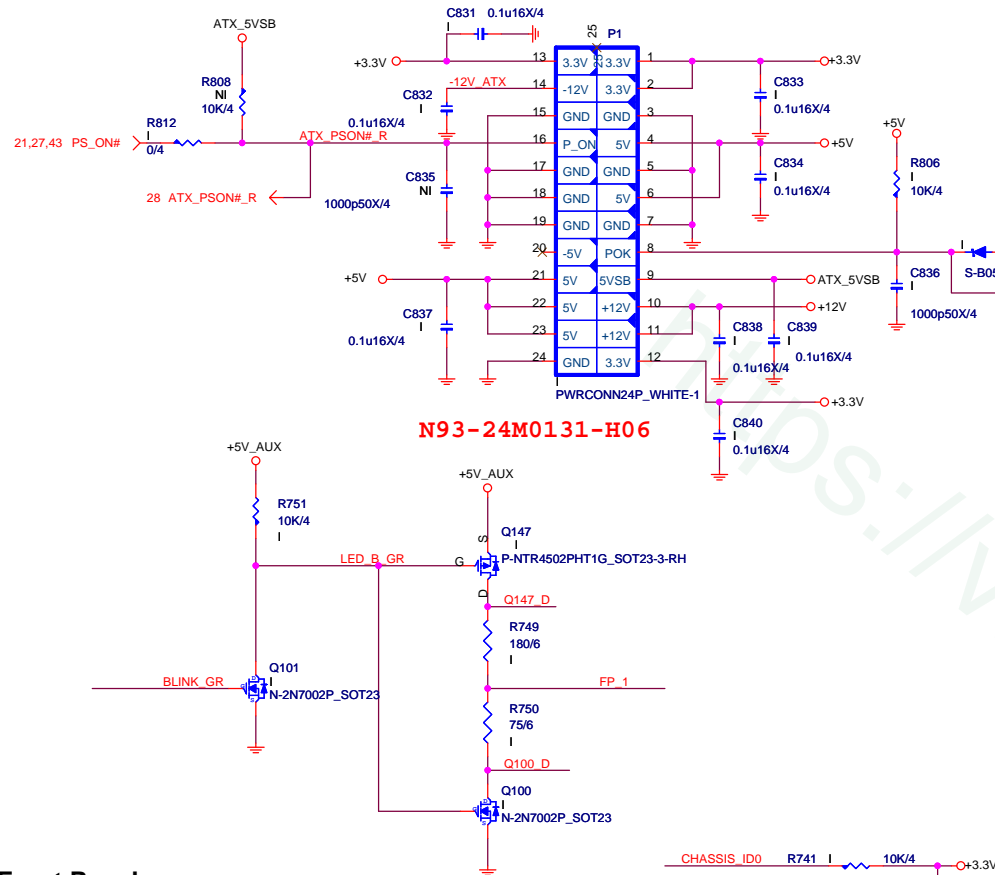
HP Restricted Secret



MICRO-STAR INT'L CO.,LTD		
HP SCH P/N: 718773-000(MSI MS-7860)		
Size	Document Description	Rev
Custom	PCH & ME Core Power	A
Date:	Sheet 43 of 56	

ATX Power Connector / Front Panel / LED/DSW

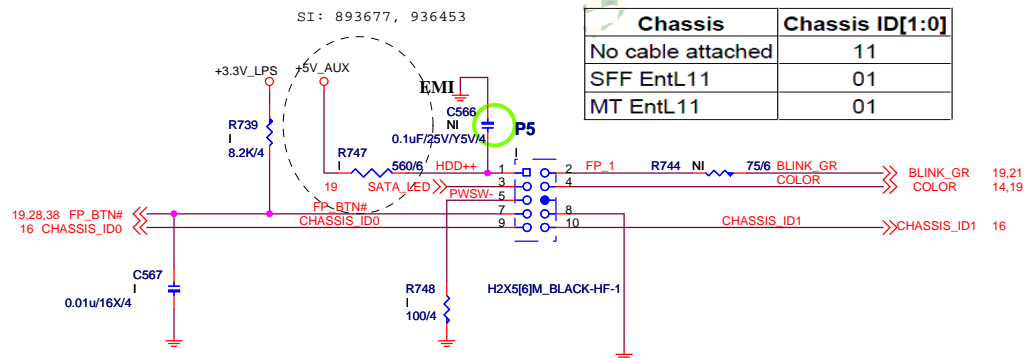
ATX CONNECTOR



N93-24M0131-H06

Front Panel

PN:N31-2051641-H06

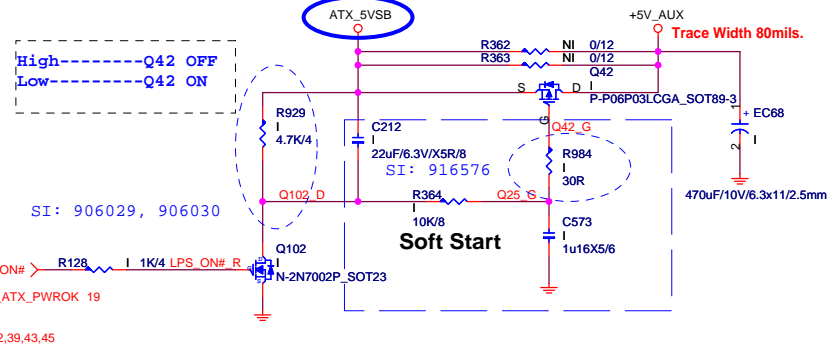


CHASSIS ID[1:0]

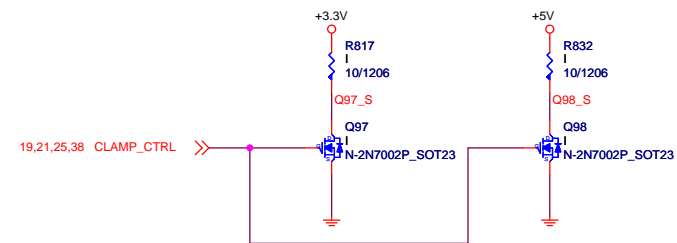
Chassis	Chassis ID[1:0]
No cable attached	11
SFF EntL11	01
MT EntL11	01

+5V AUX Power Switch

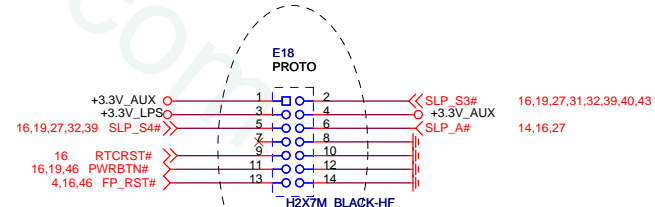
Tune ATX_5VSB inrush current to 2A from 4A



BLEED-OFF CIRCUIT



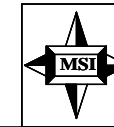
SI: 892659/892663



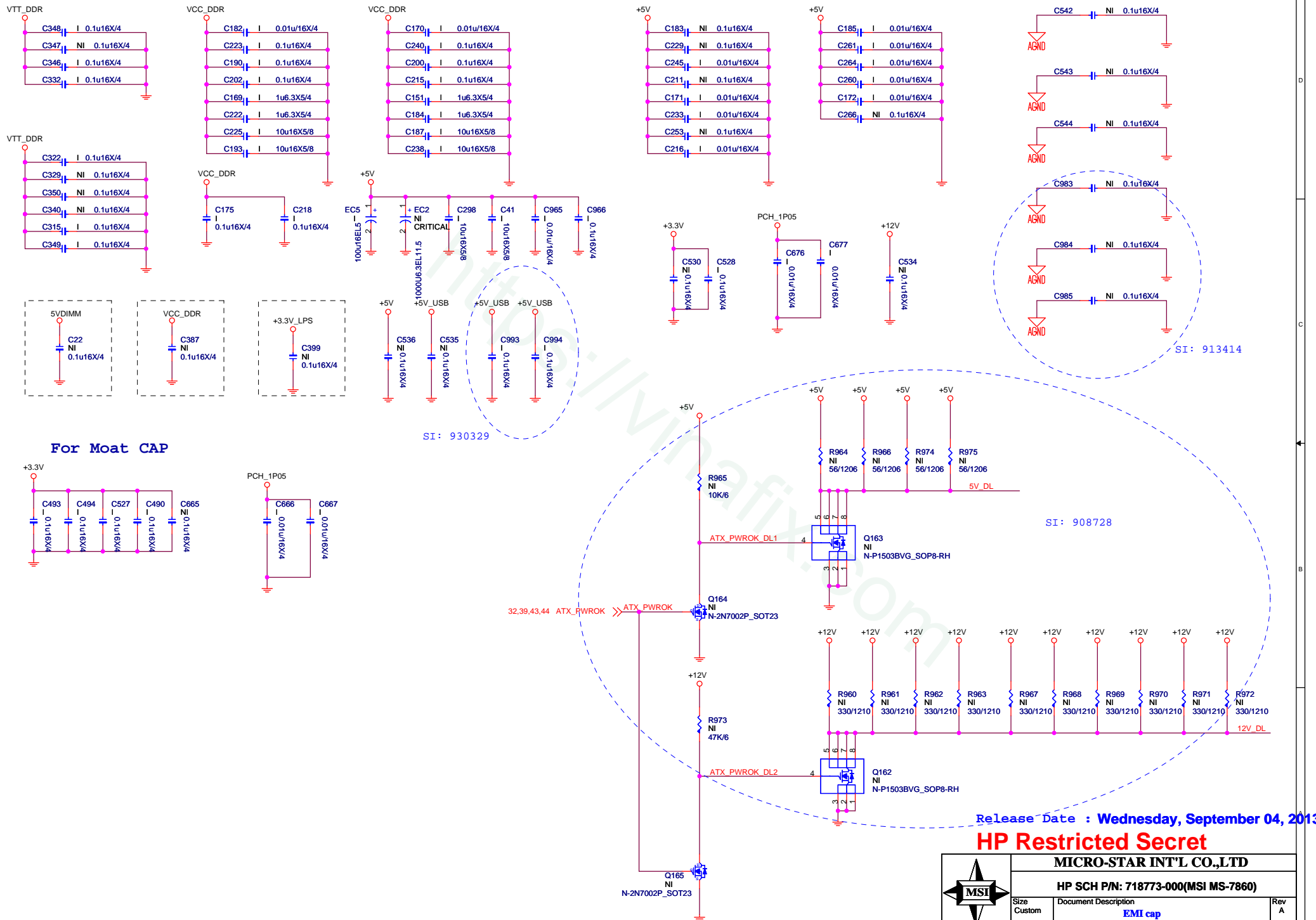
Release Date : Wednesday, September 04, 2013

HP Restricted Secret

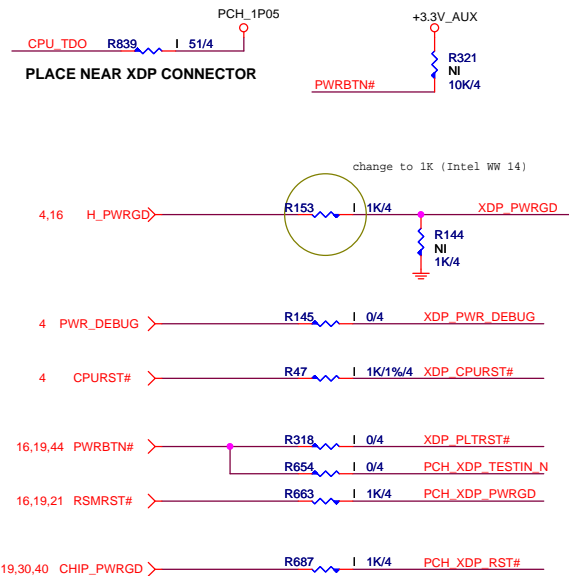
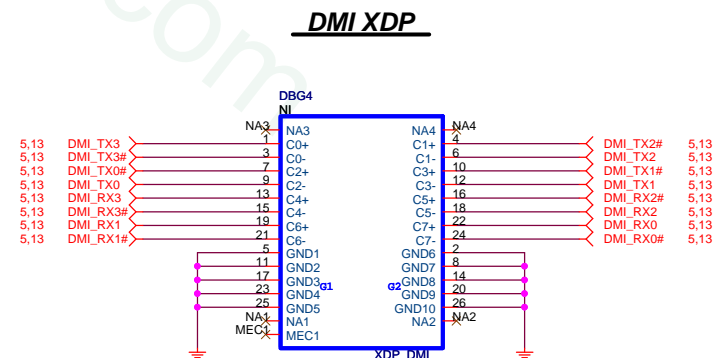
MICRO-STAR INT'L CO.,LTD	
HP SCH P/N: 718773-000(MSI MS-7860)	
Size Custom	Document Description
ATX/F_Panel/EMI	
Date:	Rev A



EMI CAPs



4 H_CFG[19..0] ↔ H_CFG[19..0]

DBG1
PROTO

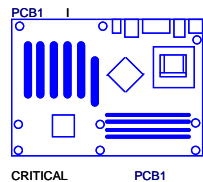
HP Restricted Secret



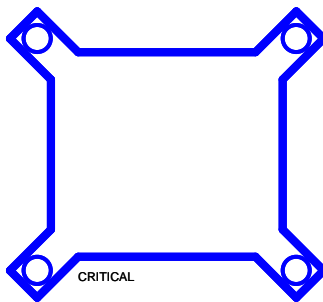
HP SCH P/N: 718773-000(MSI MS-7860)

Size Custom	Document Description CPU/PCH/DMI XDP	Rev A
Date:	Sheet 46 of 56	

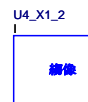
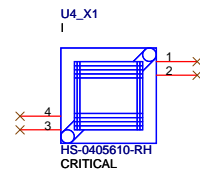
Manual Parts



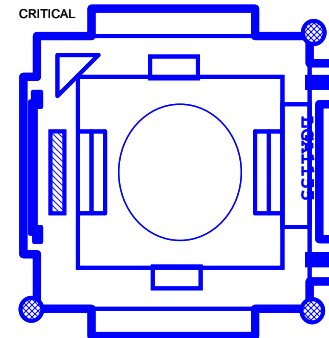
XU1_X2
E93-0000099-A21



E93-0000099-A21
AVL:E22-B009010-C22

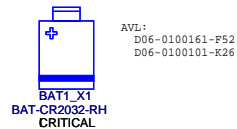


XU1_X1
CPU SOCKET
CRITICAL



E21-AC71010-L06
AVL:E21-7826010-F02

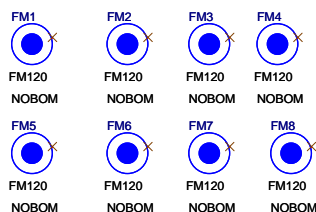
Simulation



AVL:
D06-0100161-P52
D06-0100101-K26

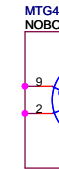
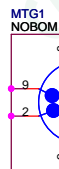
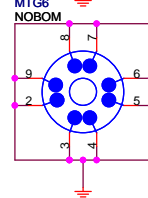
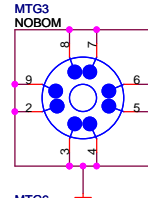
D06-0100101-P01

Optics Orientation Holes

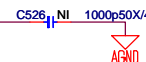


Mounting Holes

Modify for factory request.



HOLES_4S_HP_D7_2



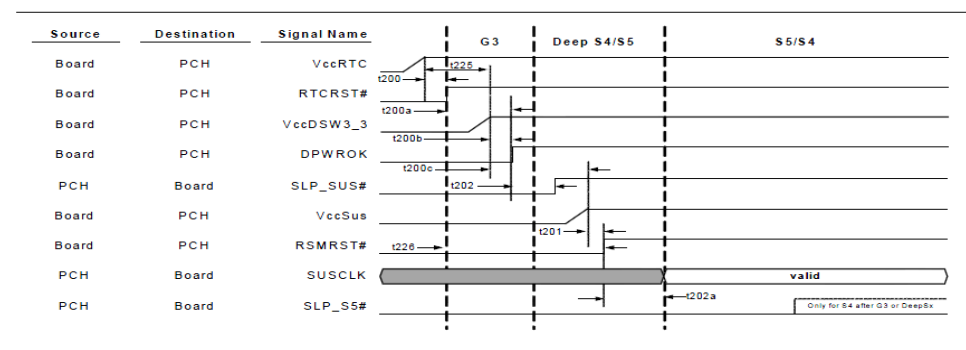
Release Date : Wednesday, September 04, 2013

HP Restricted Secret

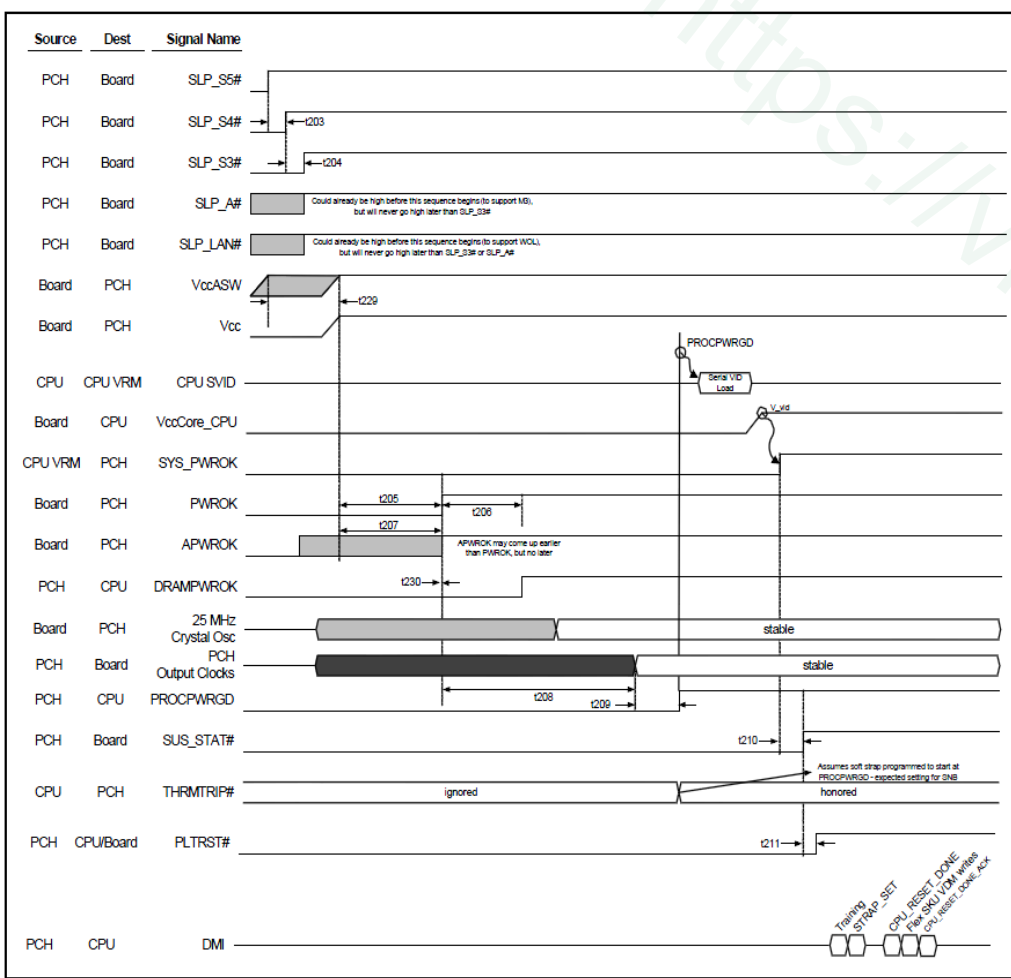


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HP SCH P/N: 718773-000(MSI MS-7860)		
Size Custom	Document Description Manual & Option Parts	Rev A
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G3 w/RTC Loss to S4/S5 (With Deep Sx Support) Timing Diagram



S5 to S0 Timing Diagram



G3-S5

ATX_5VSB

+3.3V_LPS

SLP_SUS#

LPS_ON#

+5V_AUX

+3.3V_AUX

RSMRST#

S5-S0

PWBTIN#

PWBTOUT#

SLP_S5/S4/S3

PSON#

+12V/+5V/+3.3V

VCC1_5/VCC_DDR

PCH_1P05

CHIP_PWRGD

MEM_PWRGD

H_PWRGD

VCCCP

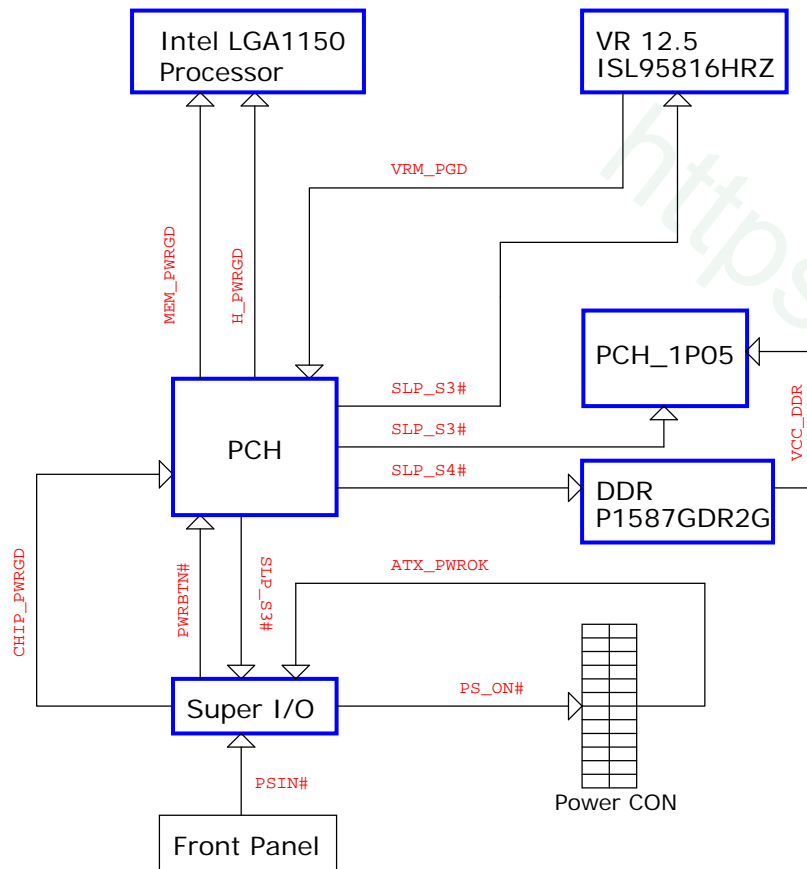
PLTRST#

Release Date : Wednesday, September 04, 2013

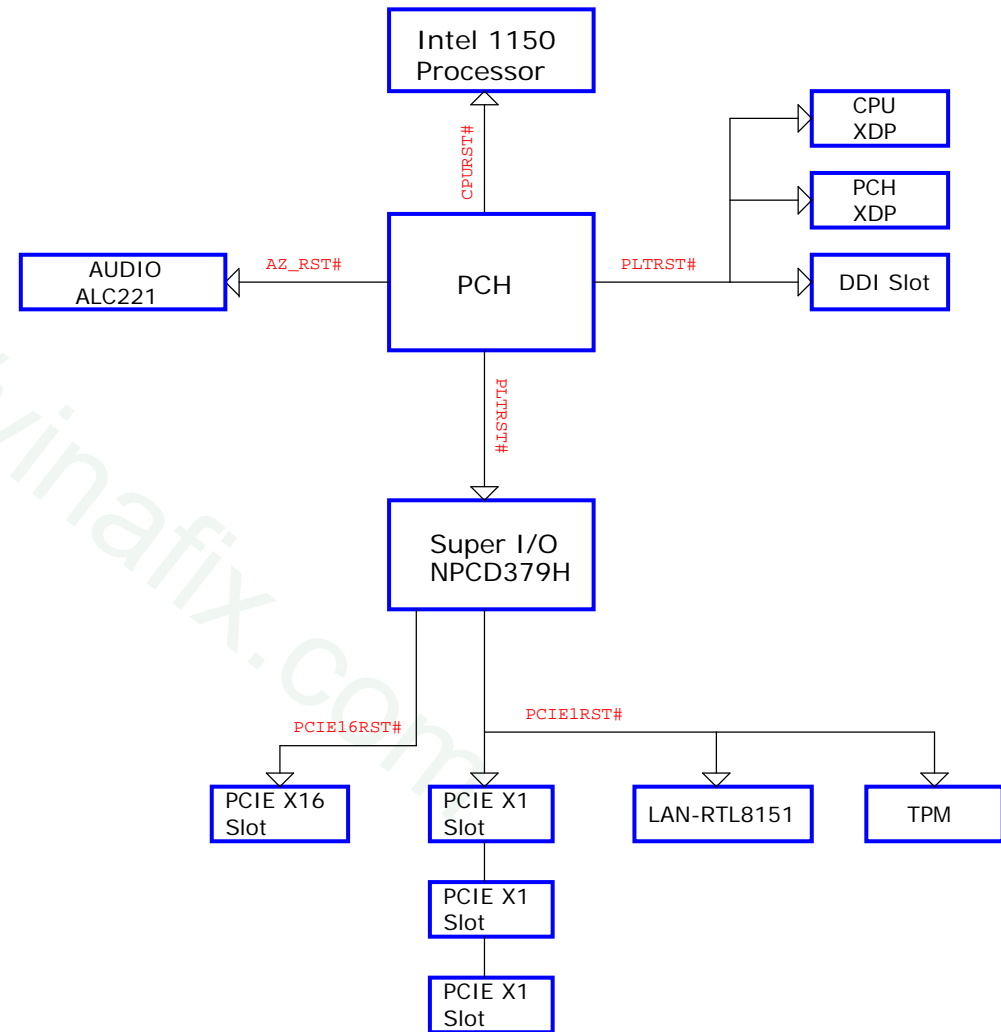
HP Restricted Secret

MICRO-STAR INT'L CO.,LTD		
HP SCH P/N: 718773-000(MSI MS-7860)		
Size Custom	Document Description PON	Rev A
Date:	Sheet 48 of 56	

PWROK MAP



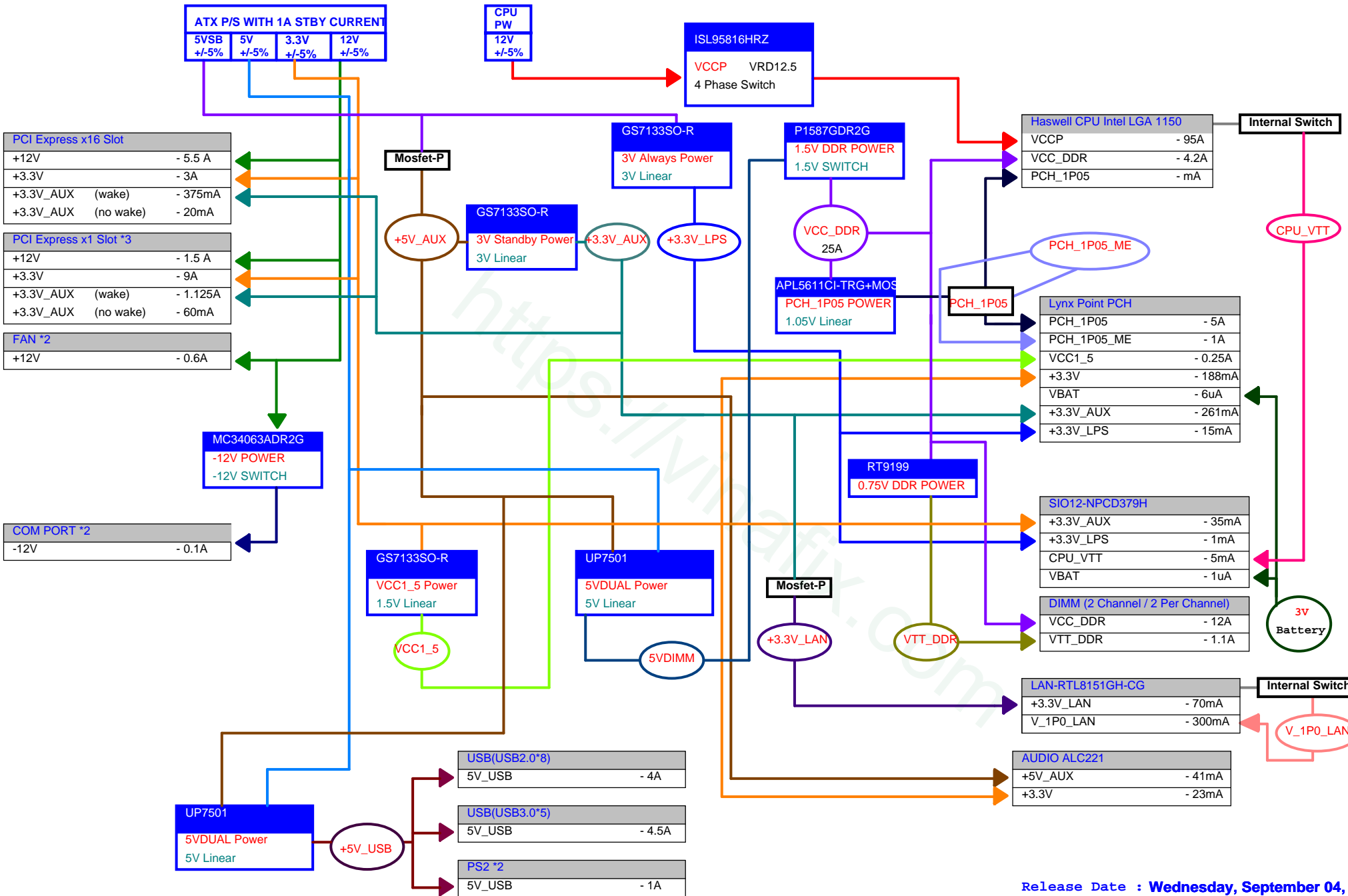
RESET MAP



Release Date : Wednesday, September 04, 2013

HP Restricted Secret

		MICRO-STAR INT'L CO.,LTD	
		HP SCH P/N: 718773-000(MSI MS-7860)	
Size Custom	Document Description Pwrok/Reset	Rev A	
Date:		Sheet 49 of 56	



Release Date : Wednesday, September 04, 2013

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	MICRO-STAR INT'L CO.,LTD		
	HP SCH P/N: 718773-000(MSI MS-7860)		
	Size Custom	Document Description Power Map	Rev A
Date:	Sheet 50 of 56		


PCH

GPIO	I/O/NC	Power	Tol	Default	MB Function
GPIO[0]	I/O	Main	3.3V	GPI	FRONT_USB_P24_DET#
GPIO[1]	I/O	Main	3.3V	GPI	PCH_GPIO1
GPIO[2]	I/O	Main	5V	GPI	PCH_GPIO2
GPIO[3]	I/O	Main	5V	GPI	PCH_GPIO3
GPIO[4]	I/O	Main	5V	GPI	PCH_GPIO4
GPIO[5]	I/O	Main	5V	GPI	PCH_GPIO5
GPIO[6]	I/O	Main	3.3V	GPI	IO_SMI#
GPIO[7]	I/O	Main	3.3V	GPI	PCH_GPIO7
GPIO[8]	I/O	Resume	3.3V	GPO	PCH_GPIO8
GPIO[9]	I/O	Resume	3.3V	Native	USB_OCP#5
GPIO[10]	I/O	Resume	3.3V	Native	USB_OCP#6
GPIO[11]	I/O	Resume	3.3V	Native	PCH_SMBALERT#
GPIO[12]	I/O	Resume	3.3V	Native	LAN_DISABLE#
GPIO[13]	I/O	Resume	3.3V	GPI	INT_USB_P151_DET#
GPIO[14]	I/O	Resume	3.3V	Native	GPIO14
GPIO[15]	I/O	Resume	3.3V	GPO	PCH_GPIO15
GPIO[16]	I/O	Main	3.3V	GPI	PCH_GPIO16
GPIO[17]	I/O	Main	3.3V	GPI	PCH_GPIO17
GPIO[18]	I/O	Main	3.3V	Native	PCH_GPIO18
GPIO[19]	I/O	Main	3.3V	GPI	PCH_GPIO19
GPIO[20]	I/O	Main	3.3V	Native	PCIECLKREQ2#
GPIO[21]	I/O	Main	3.3V	GPI	FRONT_AUD_DET#
GPIO[22]	I/O	Main	3.3V	GPI	INT_USB_P150_DET#

GPIO[23]	I/O	Main	3.3V	Native	LDRQ1#
GPIO[24]	I/O	Resume	3.3V	GPO	PCH_GPIO24
GPIO[25]	I/O	Resume	3.3V	Native	BRD_ID2
GPIO[26]	I/O	Resume	3.3V	Native	PCH_GPIO26
GPIO[27]	I/O	DSW	3.3V	GPI	PCH_LAN_WAKE#
GPIO[28]	I/O	Resume	3.3V	GPO	PCH_GPIO28
GPIO[29]	I/O	Resume	3.3V	Native	SLP_WLAN#
GPIO[30]	I/O	Resume	3.3V	GPI	PCH_SUSWARN#
GPIO[31]	I/O	DSW	3.3V	GPI	PCH_GPIO31
GPIO[32]	I/O	Main	3.3V	GPO	PCH_GPIO32
GPIO[33]	I/O	Main	3.3V	GPO	PCH_GPIO33
GPIO[34]	I/O	Main	3.3V	GPI	PCH_GPIO34
GPIO[35]	I/O	Main	3.3V	GPO	BRD_REV0
GPIO[36]	I/O	Main	3.3V	GPI	PCH_GPIO36

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PCH

GPIO	I/O/NC	Power	Tol	Default	MB Function
GPIO[37]	I/O	Main	3.3V	GPI	PCH_GPIO37
GPIO[38]	I/O	Main	3.3V	GPI	CHASSIS_ID0
GPIO[39]	I/O	Main	3.3V	GPI	BRD_ID1
GPIO[40]	I/O	Resume	3.3V	Native	USB_OCP#1
GPIO[41]	I/O	Resume	3.3V	Native	USB_OCP#2
GPIO[42]	I/O	Resume	3.3V	Native	USB_OCP#3
GPIO[43]	I/O	Resume	3.3V	Native	USB_OCP#4
GPIO[44]	I/O	Resume	3.3V	Native	PCIECLKREQ5#
GPIO[45]	I/O	Resume	3.3V	Native	PCH_GPIO45
GPIO[46]	I/O	Resume	3.3V	Native	PCH_GPIO46
GPIO[48]	I/O	Main	3.3V	GPI	CHASSIS_ID1
GPIO[49]	I/O	Main	3.3V	GPI	PCH_GPIO49
GPIO[50]	I/O	Main	3.3V	GPI	PCH_GPIO50
GPIO[51]	I/O	Main	3.3V	GPO	PCH_GPIO51
GPIO[52]	I/O	Main	3.3V	GPI	PCH_GPIO52
GPIO[53]	I/O	Main	3.3V	GPO	PCH_GPIO53
GPIO[54]	I/O	Main	3.3V	GPI	BOOT_BLK_EN#
GPIO[55]	I/O	Main	3.3V	GPO	PCH_GPIO55
GPIO[57]	I/O	Resume	3.3V	GPI	PCH_GPIO57
GPIO[58]	I/O	Resume	3.3V	Native	SML1CLK
GPIO[59]	I/O	Resume	3.3V	Native	USB_OCP#0
GPIO[60]	I/O	Resume	3.3V	Native	PCH_SML0ALERT#

GPIO[61]	I/O	Resume	3.3V	Native	PRNTER_DET#
GPIO[62]	I/O	Resume	3.3V	Native	SUS_CLK
GPIO[63]	I/O	Resume	3.3V	Native	SLP_S5#
GPIO[64]	I/O	CORE	3.3V	Native	CLKOUTFLEX0
GPIO[65]	I/O	CORE	3.3V	Native	CLKOUTFLEX1
GPIO[66]	I/O	CORE	3.3V	Native	CLKOUTFLEX2
GPIO[67]	I/O	CORE	3.3V	Native	CLKOUTFLEX3
GPIO[68]	I/O	CORE	3.3V	GPI	FRONT_USB_P26_DET#
GPIO[69]	I/O	CORE	3.3V	GPI	COMM_B_DET#
GPIO[70]	I/O	CORE	3.3V	GPI	BOOT_BLK_REC#
GPIO[71]	I/O	CORE	3.3V	GPI	BRD_ID0
GPIO[72]	I/O	DSW	3.3V	Native	PCH_GPIO72
GPIO[73]	I/O	Resume	3.3V	Native	BRD_REV1
GPIO[74]	I/O	Resume	3.3V	Native	PCH_SML1ALERT#
GPIO[75]	I/O	Resume	3.3V	Native	SML1DATA

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Pin	Default Function / Alternate Functions	Buffer Type	Buffer Power Wells	Motherboard Function
1	CLAMP_CTRL	OD _S	VS _{B3}	BLEED OFF CIRCUIT
2	SLP_S4#	IN _{TS4}	VS _{B3}	SLP_S4#
3	SLP_S5#	IN _{TS4}	VS _{B3}	SLP_S5#
4	SLP_S3#	IN _{TS4}	VS _{B3}	SLP_S3#
5	SIOPME#	OD _S O _{4B}	VS _{B3}	RI#
6	RSMRST#	O ₃₁₆	VS _{B3}	RSMRST#
7	PME_IN#	IN _{TS}	VS _{B3}	PME status
8	BLINK_OR	O ₂₀₂₀	VS _{B3}	Power LED driver
9	COLOR	O ₂₀₂₀	VS _{B3}	Power LED driver
10	VSS	I	GND	GND
11	PWRGD_OUT	OD _S	VS _{B3}	PWRGD_140ms
12	PS_ON#	OD _S	VS _{B3}	PS_ON#
13	TACH1	IN _{TS}	VDD3	SYS_FAN_TACH
14	CLOCKI32	IN _{TS}	VS _{B3}	SUS_CLK_IO
15	3V_AUX_SLOT_ON	O _{4B}	VS _{B3}	3V_AUX_SLOT_ON
16	VS _{B3}	I	PWR	VS _{B3}
17	VCORF	I	N/A	VCORF
18	LDRG#	O _{PC1}	VDD3	LDRG#
19	LAD3	IN _{PC} /O _{PC1}	VDD3	LAD3
20	LAD0	IN _{PC} /O _{PC1}	VDD3	LAD0
21	LAD2	IN _{PC} /O _{PC1}	VDD3	LAD2
22	VSS	I	PWR	GND
23	LAD1	IN _{PC} /O _{PC1}	VDD3	LAD1
24	SER_IRQ	IN _{PC} /O _{PC1}	VDD3	SERIRQ
25	PCI_RESET#	IN _{PC1}	VDD3	PLTRST#
26	PCI_CLK	IN _{PC1}	VDD3	33MHz
27	LFRANE#	IN _{PC1}	VDD3	LFRANE#
28	VS _{B3}	I	PWR	VS _{B3}
29	OPRST3#	O ₁₄	VS _{B3}	PCIE_X16 RESET#
30	INTRUDER#	IN _{TS}	V _{BAT}	HOOD_SENSE#
31	5V_USB_CTRL	O _{4B}	VS _{B3}	5V_USB_EN
32	HDLOCK#	OD ₁₂	VDD3	HOOD_LOCK#
33	GPIO01	IN _{TS} /OD _S /O _{4B}	VS _{B3}	
34	HDUNLOCK#	OD ₁₂	VDD3	HOOD_UNLOCK#
35	HD_LED_IN#	IN _{TS}	VDD3	Hard Drive LED Input
36	CPU_PRNT1#	IN _{TS1}	V _{BAT}	CPU detection
37	VBAT	I	PWR	

38	12V_VSB_COMP	IN _{COMP2}	VS _{B3}	
39	COMP_IN3	IN _{COMP3}	VS _{B3}	
40	COMP_IN1	IN _{COMP1}	VS _{B3}	5V voltage monitor
41	COMP_IN2	IN _{COMP2}	VS _{B3}	12V voltage monitor
42	AVCC	I	PWR	AVCC
43	AD1	IN _{PC} /O _{PC1}	VDD3	AD1
44	AD2	IN _{PC} /O _{PC1}	VDD3	AD2
45	AD3	IN _{PC} /O _{PC1}	VDD3	AD3
46	FSPI_STR	IN _{TS}	AVCC	FSPI_STR
47	AGND	I	GND	AGND
48	PWBTOUT#	IN _{TS4}	VLPS	PWBTOUT#
49	PWBTIN#	IN _{TS4}	VLPS	PWBTIN#
50	LPS_WAKE	IN _{TS}	VLPS	LPS_WAKE
51	LPS_PHY#	O _{4B}	VLPS	LPS_PHY#
52	LPS_ON#	O _{4B}	VLPS	LPS_ON#
53	VLPS	I	PWR	VLPS
54	VTT	I	PWR	VTT
55	THERMTRIP#	IN _{AGTL}	VTT	THERMTRIP#
56	TSI_SCL	IN _{TS} /O _{TS1}	VTT	TSI_SCL
57	PROCHOT1#	IN _{AGTL} /OD _{AGTL24}	VTT	PROCHOT1#
58	PECI	IN _{PEC} /O _{PEC1}	VTT	PECI
59	PROCHOT2#	IN _{AGTL} /OD _{AGTL24}	VTT	PROCHOT2#
60	VSS	I	PWR	GND
61	PWM2	OD ₁₂ O _{S/12}	VDD3	SYS-FANPWM_REAR
62	HMSCL	IN _{SM} /OD _S	VS _{B3}	HMSCL
63	PWM1	OD ₁₂ O _{S/12}	VDD3	SYS-FANPWM_FRONT
64	HMSDA	IN _{SM} /OD _S	VS _{B3}	HMSDA
65	HD_LED_OUT	OD ₁₆	VS _{B3}	Hard Drive LED Output
66	WAKE_OUT#	OD ₁₂ O _{S/12}	VS _{B3}	Wake Disable Output
67	GPIO15(EV6#)	IN _{TS}	VS _{B3}	PCI_Express_Wake#
68	AMP_ON	O _{4B}	VS _{B3}	AMP_ON
69	AMP_ON#	O _{4B}	VS _{B3}	AMP_ON#
70	OPRST2#	O _{14/14}	VS _{B3}	PE_RST#_OUT
71	12V_PG_25MS	OD _S	VS _{B3}	12V_PG_25MS
72	KBDRST#	IN _{TS} /OD ₁₄	VDD3	KBDRST#
73	AUDIO_BEEP	O _{4B}	VS _{B3}	DIAG Beep
74	TACH2	IN _{TS}	VDD3	TACH2
75	VS _{B3}	I	PWR	VS _{B3}
76	KBDAT	IN _{TS} /OD ₁₄	VDD3	KBDAT
77	MDAT	IN _{TS} /OD ₁₄	VDD3	MSDATA
78	SLIN_ASTRB#	OD ₁₄ O _{14/14}	VDD3	RSLIN#
79	KBCLK	IN _{TS} /OD ₁₄	VDD3	KBCLK
80	MCLK	IN _{TS} /OD ₁₄	VDD3	MCLK
81	PD3	IN _{TS} /O _{14/14}	VDD3	PD3
82	PD4	IN _{TS} /O _{14/14}	VDD3	PD4

83	INIT#	OD ₁₄ O _{14/14}	VDD3	INIT#
84	VSS	I	PWR	GND
85	PD1	IN _{TS} /O _{14/14}	VDD3	PD1
86	PD6	IN _{TS} /O _{14/14}	VDD3	PD6
87	PD0	IN _{TS} /O _{14/14}	VDD3	PD0
88	PD2	IN _{TS} /O _{14/14}	VDD3	PD2
89	PD7	IN _{TS} /O _{14/14}	VDD3	PD7
90	PD5	IN _{TS} /O _{14/14}	VDD3	PD5
91	STB_VWRITE#	OD ₁₄ O _{14/14}	VDD3	RSTB#
92	ERR#	IN _{TS}	VDD3	RERR#
93	VS _{B3}	I	PWR	VS _{B3}
94	AFD_DSTRB#	OD ₁₄ O _{14/14}	VDD3	RAFD#
95	PE	IN _{TS}	VDD3	RPE
96	GA20	IN _{TS} /O _{14/14}	VDD3	GA20
97	ACK#	IN _{TS}	VDD3	RACK#
98	SLCT	IN _{TS}	VDD3	RSCT
99	BUST_WAIT#	IN _{TS}	VDD3	RBUSY
100	TACH3	INTS	VDD3	TACH3
101	SMB1SDA	SW _{SM}	VDD3	SMB_DATA_MAIN
102	PWRGD_PS	IN _{TS4}	VS _{B3}	PWROK_PS
103	SMB2SDA	SW _{SM}	VDD3	SMB_DATA_RESUME
104	PWRGD_O2#	OD _S	VS _{B3}	PWRGD_50MS#
105	PWM3#	OD ₁₂ O _{S/12}	VDD3	PSU-FANPWM
106	5V_USB_MAIN#	OD _S	VS _{B3}	5V_USB_MAIN#
107	PWRGD_O1	OD _S	VS _{B3}	PWRGD_30MS
108	VSS	I	PWR	GND
109	SMB1SCL	SW _{SM}	VDD3	SMB_CLK_MAIN
110	SMB#	OD _S	VDD3	IO_SMB#
111	SMB2SDL	SW _{SM}	VDD3	SMB_CLK_RESUME
112	DSR1#	IN _{TS}	VDD3	DSRA#
113	RI1#	IN _{TS}	VDD3	RIA#
114	CTS1#	IN _{TS}	VDD3	CTSA#
115	DCD1#	IN _{TS}	VDD3	DCDA#
116	SIN1	IN _{TS}	VDD3	SINA
117	RTS1#	O _{4B}	VDD3	RTSA#
118	DTR#_BOUT1	O _{4B}	VDD3	DTRA#
119	SOUT1	O _{4B}	VDD3	SOUTA
120	DCD2#	IN _{TS}	VDD3	DCDB#
121	SOUT2	O _{4B}	VDD3	SOUTB
122	VS _{B3}	I	PWR	VS _{B3}
123	DTR#_BOUT2	O _{4B}	VDD3	DTRB#
124	RI2#	IN _{TS}	VDD3	RIB#
125	RTS2#	O _{4B}	VDD3	RTSB#
126	SIN2	IN _{TS}	VDD3	SINB
127	DSR2#	IN _{TS}	VDD3	DSRB#
128	CTS2#	IN _{TS}	VDD3	CTSB#

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2012/10/22

PAGE 7: Changed R436 from 3.16K ohm to 2.67K ohm.(SI number: 892595/892596)

PAGE 16: Modified R721 and R231 pull-up well from +5V_AUX to ATX_5VSB.(SI number: 892601/892602)

PAGE 20: Modified J68 to separated connector J66 and J67(HP spec change).(SI number: 892604/892605)

PAGE 22: Modified DP to DDI connector (HP spec change).

Add: J34.

Remove: C120,C117,C115,C110,C100,C108,C95,C98,C96,C99,C80,Q26,F2,R194,R199,
RN29,RN30,RN31,RN32,R421,R188,R210,R183,C132,R530,Q30,R196,
R278,Q28,R201,R206,U16,U45,U30,Q31,Q32,R211,R212,C149,C159,C165,C171,
C79,C71,R193,J64,L13,L12,L9,L11(SI number: 892607/892609)

PAGE 23: Modified DP header to DVID connector (HP spec change).

Remove: C121,C118,C111,C116,C101,C109,C97,C102,C103,C104,R202,R214,RN33,RN34,
RN35,RN36,L32,L33,L10,L34,R423,R215,R204,R185,C133,R544,Q51,R205,R279,
Q55,U17,U15,U39,Q40,R224,Q56,R222,C150,C162,C166,C174,C82,Q52,R217,R216,
F3,C83,C72,R223,P55

Add: C66,C69,C56,C57,C58,C61,C51,C53,R233,Q34,C81,U21,C76,C75,C84,U14,U6,
R181,R164,R173,R138,R140,R172,R103,R112,Q33,R170,R162,Q20,Q29,R166,R232,
RN21,RN22,RN23,RN24,L7,L8,L6,L5,R242,R276,R297,R299,D75,F1,FB4,C77,C1,
C2,R238,C168,J65(SI number:892611/892614)

PAGE 24: Modified J69 to J65(HP spec change).(SI number: 892615/892617)

PAGE30:Change audio mapping to follow reference circuit. C450
change to connect from ul3 pin17 to pin15: C451 change to
connect from ul3 pin16 to pin14 (SI number: 892619/892622)

PAGE30:Modify audio circuit by audio vendor review. FB12
connect to +3.3V,U19 pin9 connect to R918 and R844 (SI
number: 892625/892626)

PAGE31:Modify audio circuit by audio vendor review.
R413,U20,R396,C471,R415 changed to NI; added FB6,D78;
deleted D24 (SI number: 892625/892626)

PAGE32:Add USB switch control circuit
Added R530,Q92 (SI number: 892628/892629)

PAGE33:Deleted USB charging circuit by HP changed specification .
Deleted C181,C188,Q60,Q59,C186,C196,R725,R740,R112,R103,R299,R87,
C51,U38,R77,R232,R110,R118,U63,R893,R895,R892,R895,R892,C586,
R730,R138,R233,Q103,Q104 (SI number: 892633/892634)

PAGE34:Deleted USB P151 Header circuit by HP changed specification .
Deleted RN63,L4,RN46,L3,D3,C21,P151,C630 (SI number: 892635/892637)

PAGE35:Deleted USB2.0x2 connector and added USB3.0x2+USB2.0x2
connector circuit by HP changed specification . Deleted
J891,J82,JV81,RN60,L26,
RN61,L25,RN40,L19,RN41,L47,RN42,L50,RN43,
L48,C677,C278,C271,C266,C263,U27,U28,D30,C345; added
J10,JV10,D3,C21,RN63,L4,RN46,L3 (SI number: 892639/892640)

PAGE36:Added USB P152 Header circuit by HP changed specification . Added
U27,U28,D30,C345,C278,C271,RN42,L50,RN40,L19,RN60,L26,C726,P152(SI number: 892643/892645)

PAGE38:Modify Fan circuit ;EC6 and C204 changed from NI to I (SI number: 892646/892649)

PAGE39:Added EC cap for DDR power by power team suggestion ;Added EC27(SI number: 892651/892654)

PAGE40:Modify CPU power circuit by power team suggestion ;R104,R67,R96,R49 changed
from 6.2K to 6.34K ohm (SI number: 892656/892658)

PAGE44:Modify APS header circuit ;E18 pin 4 changed from SLP_S5# to +3.3V_AUX.
(SI number: 892659/892663)

2012/10/23

PAGE16:Reserve C540 for EMI.(SI number: 892666/892667)

PAGE20:Change FB13, FB14, FB15,FB16 from 0 ohm to 33 ohm for EMI.(SI number:892666/892667)

PAGE20:Add D61 for EMI.(SI number: 892666/892667)

PAGE24: Delete D10, D11 for EMI.(SI number: 892666/892667)

2012/10/24

PAGE 14: Modify R807 and R371 from 10k ohm to 499 ohm by Intel review.(SI number:893429)

PAGE 16: Rename PCIECLKREQ#5 to PCH_GPIO44 by Intel review.(SI number:893434)

PAGE 16: Rename PCIECLKREQ#2 to PCH_GPIO20 and modify R367 to NI by Intel review.(SI number:893434)

PAGE 24: Modify R285 and R292 from I to NI by Intel review.(SI number:893437)

PAGE 28: Add R920, R921,modify R900 to 0ohm, modify Q135 to 2N7002 by Intel review.(SI number:893435)

PAGE 21: Modify C445,C446 and C449 from NI to I by SIO vendor review.(SI number:893439)

PAGE 30: Modify C455 from 0.1uF to 10uF by audio vendor review.(SI number:892625)

2012/10/25

PAGE 42: Power team suggest to modify C647,C649,C644,C646,C648,C650,C652,
C653,C654,C655 from I to NI.(SI number:893441)

PAGE 17: Delete C683,C524 and add C960,C961,C962 by Intel review.(SI number:893898)

PAGE 43: Add C963,C964 by Intel review.(SI number:893898)

PAGE 16: Modify R738 from 2.2k ohm to 10k ohm,
modify R120 from 100k ohm to 10k ohm and modify to NI by Intel review.(SI number:893898)

2012/10/26

PAGE 44: Modify R747 from 75 ohm to 180 ohm and connect to +5V_AUX.(SI number:893677)

2012/10/30

PAGE 38: Delete 3/4 pin system fan colay circuit:
Delete: R36,C23,R499,R497,U67,R283,Q80,R236(SI number:896536)

PAGE 13: Modified PCIE clock mapping by HP requirement:
Connect PE6_CLK to J31, PE5_CLK to J32, PE0_CLK to J33.(SI number:894512)

PAGE 43: Modify EC1 from 270uF to 100uF by power team suggestion.(SI number:895385)

2012/11/01

PAGE 05: Modify DVI port mapping port D by HP requirement.(SI number: 894794)

2012/11/02

PAGE 45: Add C965, C966 for EMI.(SI number:896534)

2012/11/09

PAGE 23/24: Separate J65 (DVI+VGA) into J65 (DVI) and J69 (VGA).(SI number:892615/892617)

PAGE 14: Modified net PCH_GPIO1 to DC_DET# and connected to J34.(SI number:896525)

PAGE 40: Modified CPU PWM solution from NCP81102MNTXG to ISL95816HRZ.
Delete: R34,R1,C19,R31,R14,R15,C5,C18,R5,R13,R3,R16,C7,R4,R24,R30,C16,R22,R11,C17,R840,R7,R6,C15,R56,R55,R99,
R100,R131,RT3,R114,C40,R130,R91,R92,R74,R44,C26,R9,R32,C3,R63,R69,R62,C31,R90,R113,R122,R133,C46,
R81,R105,R104,C43,C44,R59,R70,R67,C34,C32,R82,R94,R98,C42,C38,R53,C24,C25,R49,R20,R28,R27,R39,RT1,
C12,C11,R19,R21,R10,C6,R124,R68,R108,R41,R107,R58,R89,R33,C20,R42,R35,R558.
Add: R70,R82,C23,R107,R58,R27,R45,R36,R105,C25,R87,C24,C34,C17,R110,R89,C42,C38,R53,R63,R55,R77,R92,C40,
R99,C46,R104,R30,C43,C12,R4,C4,R1,R24,R9,R14,R29,R91,C26,R2,C3,R6,C7,R3,R49,R15,R22,R16,R31R20,R8,
R44,R43,R42,R39,R19,R25,R28,C10,R100,R111,R108,C18,R52,R62,R90,R68,R94,R81,R61,C29,R59,R67,R69,R66,
R32,R74,R98,RT1,R21,C9,R23,C8,C6,R5,C11,R18,C13,R13,RT3.(SI number:896517)

2012/11/13

PAGE 31: Add R452, R453 and C524 and connect to pin 2 of P23 by HP suggestion.(SI number:)

PAGE 45: Add C183,C229,C245,C211,C171,C233,C253,C216,C185,C261,C264,C260,C172,C266,C530,C528,C676,C677,C534
by HP suggestion.(SI number:)

PAGE 47: Add C526 by HP suggestion.(SI number:)

PAGE 47: MH7 connect to GND by HP suggestion.(SI number:)

2012/11/14


PAGE 42: Modified EC24 from I to NI by power team suggestion.(SI number:898665)

PAGE 39: Add C173 by power team suggestion.(SI number:898666)

PAGE 45: Add C535, C536, C542,C543,C544 for EMI.(SI number:898667)

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PAGE 35: Separate J10 to J81 and J82 by HP spec change.(SI number:898670)

PAGE 40: Modified C24 to 4.7k ohm and modified NI to I by power team suggestion(SI number: 898673)

PAGE 22: Modify DP header to 2X10 pin by HP spec change.(SI number:898672)

Gwen/Mordred X2

2013/01/03

PAGE 29/35: The one PCB leverage proposal from MSI had been approved and will implement into EVT-2 phase. Modify J9 from RJ45+USB2.0 to RJ45+USB3.0 connector.(SI:913289)

PAGE 34: The one PCB leverage proposal from MSI had been approved and will implement into EVT-2 phase.Combine J81 and J82 USB 2.0 port to J10 USB2.0 X4 connector.(SI:913289)

PAGE 30:Rear Line in port malfunction. Modify R386 from 20k ohm to 39.2k ohm.(SI:903668,903669)

PAGE 44: UUT can not enter S5 Max Power Saving mode. Add R929 .(SI:906029,906030)

PAGE 43: There is no function for COM port.Connect Pin 8 of U35 to U5_SWC.(SI:902802)

PAGE 39: DDR power dynamic Load test is fail.
Moidy C496 from 1000pf to 470pf; Modify R247 from 2k ohm to 2.74k ohm;Modify R274 from 12k ohm to 7.68k ohm;Modify C324 from NI to I.(SI:910564,910565)

PAGE 17:amelot PCA Mordred/Gwen Schematic review bt Intel schematic review feedback .Add R932 .(SI:893898)

PAGE 31: Change front IO P23 pin2 from AGND to GND, Modify R453 to NI and R452 to I.(SI:913268)

2013/01/08

PAGE 16: A item of power on sequence signal integrity test is fail.Modify C129 from 2.2uf to luf.(SI:908764,908768)

PAGE 40: Modify HP Gwen/Mordred Cpu Power circuit to meet the test of Intel CPU power transient.
For Gwen:
Modify R32 from 4.7M ohm to 5.6M ohm.Modify R91 from 137K ohm to 110K ohm.Modify R92 from 3.83K ohm to 3.57K ohm.Modify C6 from 0.22uF to 0.47uF.
Modify C17 from 100pF to 68pF.Modify C26 from 0.01uF to 820pF(SI:905259)
Add Mordred colay parts:
PR32, PR91, PR92, PR29, PR110, PC6, PC11, PC17, PC26(SI:905260)

2013/01/14

PAGE 28: Use WAKE # signal can support OBFF function.
Modify R919 from I to N;Add Q151, Q152, Q153, R933, R934, R935, R936, R937, R951.(SI:912719)

PAGE 28: Modify Lan disable circuit to ensure same circuit with HP other projects.
Delete R900, R920, Q135 (SI:912753)

PAGE 32:+5 V_USB inrush current will cause the voltage drop.Delete Q92;
Add Q154, Q155,R938, R939, R940, C969, C970.(SI:911783,911786)

PAGE 43: +3.3V_AUX inrush current will cause the voltage drop of +5V_AUX.Modify R519 from 4.7k ohm to 20k ohm.
Add C968 and modify EC47 to NI.(SI:911788,911790)

PAGE 22: Modify DP connector circuit.
Modify P185 to PCIE X1 slot.
Delete FS2,R930,R931,R193,R174,R196,R183,R752.(SI:913444)

PAGE 16: Support SPI BIOS Quad IO Operation mode in EVT2 PCB.Modify R218, R220 to I.(SI:913300)

PAGE 24: Rise time ,fall time and pk-pk noise of D-Sub signal Integrity Items are fail.Modify L35,L36,L37,L38,L41,L51 to 33 nH.(SI:908746,908748)

2013/01/15

PAGE 36: 3 ports USB2.0 signal integrity test is fail.Modify D42,D30,L14,L15,L26 to I and modify RN55,RN56,RN60 to NI.(SI:910566,910567)

PAGE 30: Reserve this circuit to avoid ALC221 POP noise form CODE.
Delete R480,R198,R860,Q128,Q146.
Add Q160,Q161,R953,R954,R955,R956C982,D80.
Modify R953 from 1Kohm to 4.7Kohm. (SI:912682,912689)

PAGE 45: Add several stitching capacitors (layer change) in EVT2 PCB by MSI EMI engineers suggestion.
Add C983, C984 and C985. (SI:913414)

PAGE 43: Modify -12V circuit by MSI power engineer suggestion.
Add C986.
Modify EC1 to 270uF and R483 to 16.5k ohm. (SI:913414)

2013/01/28

PAGE 28: Modify +3.3V_LAN circuit to follow power design rule.
Modify R502 from 1K ohm to 30 ohm. (SI:916576)

Gwen/Mordred X3

2013/03/19

PAGE 40: Modify HP Gwen/Mordred Cpu Power circuit to meet the test of Intel CPU power transient.
Modify R3 from I to NI.
For Gwen:
Modify R91 from 110K ohm to 115K ohm.Modify C17 from 68 pF to 39 pF. (SI:905259)
For Mordred:
Modify PR91 from 113K ohm to 124K ohm. (SI:905260)

PAGE 38: Reserve TPM circuit.
Add U40,R959,R981,R957,R958,C850,C987,C988,C989,C990. (SI:929486)

PAGE 45: Reserve Dummy load circuit.
Add Q162,Q164,Q165,R960,R961,R962,R963,R964,R965,966,R967,R968,R969,R970,R971, R972,R973,R974,R975. (SI:908728)

PAGE 44: Modify +5V_AUX circuit to follow power design rule.
Add R984. (SI:916576)

PAGE 30: Reserve audio codec ALC221-VA and ALC221-VB colay circuit.
Add R976,R977,R978,R979,C991,C992. (SI:930271)

PAGE 28: Remove OBFF circuit.
Modify R919 from IN to I and delete Q151,Q152,R933,R934,R935,R951. (SI:912719)

PAGE 32: Use SLP_S4# to control USB switch IC.
Add R982 and R983. (SI:908728)

PAGE 43: Modify LDO Power circuit VCC1_5, +3.3V_AUX and +3.3V_LPS to meet the phase margin and gain margin test.
Modify C330 and C337 from NI to I. Modify C334 from 0.1uF to 0.033 uF for VCC1_5.
Modify EC47 from EL cap 1000uF to solid cap 100uF for +3.3V_AUX.
Modify R648 from 32.4K ohm to 324K ohm. Modify R638 from 10K ohm to 100K ohm for +3.3V_LPS. (SI:930329)

PAGE 45: Add several capacitors at +5V_USB by MSI EMI engineers suggestion.
Add C993 and C994 (SI:930302)


PAGE 21/30: Modify Amplifier Enable circuit to avoid ALC221 POP noise form CODE.
Add D81. Modify R953 from 4.7K ohm to 20K ohm. (SI:912682,912689)

PAGE 14: UUT shutdown after 8 error beep sounds if BBR jumper installed.
Add C995. Modify R226 from 1K ohm to 390 ohm. (SI: 924414,924417)

PAGE 14: Modify Board Rev to 01.
Modify R656 from NI to I and modify R653 from I to NI. (SI: 933025)

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Gwen/Mordred X3
2013/03/26
PAGE 46: Follow PCA spec and rename screw hole.
Rename MH1,MH2,MH3,MH4,MH5,MH6,MH7,MH8 to MTG1,MTG2,MTG3,MTG4,MTG5,MTG6,MTG7,MTG8. (SI: 932283)

PAGE 39/41/42: Follow PCA spec and modify cap size at PWM regulator high-side MOSFET drain .
Modify C31,C60,C86,C163,C196 size from 0805 to 1206. (SI: 932283)

2013/03/27
PAGE 22: Modify DP slot circuit.
Connect +5V to Pin A5 of P185. (SI: 932980)

PAGE 16/28: Modify crystal CL value according to crystal vendor test result.
Modify C942 from 27pF to 22pF. Modify C514 and C515 from 18pF to 15pF. (SI: 932989)

2013/04/09
PAGE 21: Remove the unused thermal sensor by thermal engineer suggestion.
Modify RT5,R610,C446 from I to NI. (SI: 935536)

PAGE 4: Modify thermtrip circuit according to Intel design guide.
Modify R213 from I to NI.(SI: 924414,924417)

Gwen/Mordred X4

2013/05/21
PAGE 30: Internal speaker has pop noise when UUT remove power cord.
Modify R200 to NI, Modify R733 from 20K ohm to 1K ohm,
Modify R734 from 20K ohm to 10K ohm and connect to +3.3V_AUX.
Add C996 and connect pin X of D80 to GND(SI: 943581)

PAGE 33/36: Follow PCA spec X81 pin definition to add USB2.0 port7 on P152.
Add RN64, L52 and U67. (SI: 935708)

PAGE 37: Motherboard have no PSWD jumper that makes BIOS password always be reset.
Modify JP49 from MP to I. (SI: 941138)

PAGE 43: Modify -12V circuit by msi power team engineer suggestion.
Modify C49 from 2200 pF to 1500 pF. (SI: 947863)

PAGE 1: Remove "ODM confidential" from schematic. (SI: 948604)

2013/05/27
PAGE 39: Modify DDR power circuit by msi power team engineer suggestion.
Modify R274 from 7.68K ohm to 9.53K ohm, modify R247 from 2.74K ohm to 3.74K ohm. (SI: 948994)

PAGE 40/42: Modify HP Gwen/Mordred CPU Power circuit to 3 phase support 84W.
Modify C42 and R89 from NI to I, modify R110 from 82K ohm to 100k ohm, modify R92 from 3.57K ohm to 3.6K ohm,
modify C26 from 820pf to 680pf, modify R91 from 115K ohm to 118K ohm, modify R21 from 487 ohm to 620 ohm,
modify R32 from 5.6M ohm to 6.2M ohm, Modify C6 from 0.47uF to 0.1uF, modify C11 from 0.33uF to 0.47uF,
modify C29,R94,R81,R59,R67,R69,R66,PR32,PR29,PR91,PR92,PR110,PC6,PC11,PC17,PC26,R188,C96,R194,C95,R187,C98,
U12,R244,R197,R266,Q11,Q21,Q12,R195,C109,CHOKE4,C680 to NI. (SI: 947654)

2013/05/29
PAGE 31: UUT has noise when play media file and plug in/pull out the MIC from front panel.
Reserve C997 and C998. (SI: 946837)

2013/06/10
PAGE 31: Remove retasking function.
Modify EC18 and EC23 from I to NI. Modify C997 and C998 from NI to I. (SI:946837)

PAGE 43: A item of power on sequence signal integrity test is fail.Modify R372
from 200K ohm to 1M ohm. Modify R538 from 10K ohm to 100K ohm.
Modify R536 from 29.4K ohm to 287K ohm(SI:949150)

2013/06/14
PAGE 44: The LED brightness and color looks not good on both Power LED and HDD LED.
modify R747 from 180 to 560 ohm. (SI: 936453)

PAGE 28: Disable GPIO12 function to support after G3 wake on lan.
Modify R900 from I to NI. (SI: 952714)

2013/06/14
PAGE 34/35/36/43/45: USB 2.0 R/W EMC test issue.
Modify C171,C172,C185,C216,C233,C245,C260,C261,C264,C411,C416,C423,C666,C667,C676,C677,C965 from 0.1uf and NI to 0.01uf and I.
Modify RN38,RN39,RN40,RN42,RN44,RN45,RN46,RN47,RN48,RN49,RN50,RN51,RN52,RN53,RN54,RN57,RN58,RN59,RN62,RN63 from I to NI.
Modify L43,L45,L22,L21,L42,L44,L46,L49 from NI to I.
Modify L3,L4,L28,L23,L27,L24,L16,L17,L18,L20,L50,L19 from NI to I,NI(SI: 950882)

Gwen/Mordred X5
2013/07/12
PAGE 20/45: Fix COM port ESD issue.
Modify C966 from NI to I and C766 from 100pf to varistor.(SI: 966671)

PAGE 14: Modify MB rev ID to 10
Modify R656, R632 from I to NI and modify R653, R629 from NI to I.

PAGE 30: Reserve audio codec ALC221-VA and ALC221-VB colay circuit.
Add C971,C972,C973,FB17,FB18,R987,R990,R991,R992,R993. (SI:964319)

PAGE 35/36: USB 2.0 R/W EMC test issue.
Modify L28,L23LL24,L27,L50,L19 from I,NI to NI. Modify RN62,R57,RN58,RN59,RN42,RN40 from NI to I,NI.
Modify RN51,RN52,RN53,RN54 from NI to I. Modify L14,L16,L18,L20 from NI to I (SI: 950882)

PAGE 43: Add a 30 ohm resistor on Q49 gate pin.
Add R1020. (SI:964320)

PAGE 32/33: USB3.0 HDD re-enumerate or lost intermittent.
Modify EC25,EC26,EC29,EC30,EC37 caps from 470uF to 1000uF. (SI:958227)

PAGE 21: Power LED blinks 4 times at low temperature during 11.2 strife test.
Modify R611 from 40K to 27.4K and modify R581 from 10K to 5.6K. (SI:955525)

PAGE 23: Fix DVI EMC test issue.
Modify RN21,RN22,RN23,RN24 from I to NI and modify L5,L6,L7,L8 from NI to I. (SI:964609)

PAGE 30/43: System power on - off continuity if 12V power did not connect.
Reserve D43, D82
Add Add Q166, R994, R1021 and R1022. Modify R538 from 100K to 10K, modify R536 from 287K to 29.4K,
modify R372 from 1M to 200K, modify R519 from 20K to 100K
R519 power well change to +3.3V_LPS from +5V_AUX.(SI: 961863)


Gwen/Mordred REV.A

2013/09/02
PAGE 14: Modify MB rev ID to A
Modify R629 from I to NI and modify R632 from NI to I. (SI:984315)

PAGE 46: Remove soldermask of pins for debug ports
JXDPI and DBG1 footprint changed to 2X30_XDP_CONN_TEST. (SI:984479)

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